Bowen Yuan

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Education

University of British Columbia – BASc in Engineering Physics – 4.0 Expected May 2027
Coursework: RF Integrated Circuits, Analog CMOS IC Design, Signals and Systems, Applied Solid State Physics

Skills

Software: Python, MATLAB, C++, Verilog, VHDL
Hardware: 45 nm CMOS PDK, Cadence Virtuoso Studio, ADE Explorer, Spectre, SPICE, Altium, Quartus Prime
Laboratory Equipment: Vector Network Analyzers, Spectrum Analyzers, Oscilloscopes, Logic Analyzers

Experience

RF Communications System Engineer, UBC Orbit Satellite Design May 2025 – Present

- Designed RF and mixed-signal component verification PCBs with Altium and LTspice supporting low-noise, high-reliability satellite communications hardware
- Measured and analyzed antenna gain, RF chain losses, and link budget using spectrum analyzers, vector network analyzers, and signal generators, ensuring ≥ 3 dB SNR margin at carrier
- Performed comprehensive hardware validation with thermal vacuum and vibration qualification testing, verifying RF system performance across environmental stress
- Performed root-cause analysis and FMEA to identify critical RF failure modes, and developed mitigation strategies reviewed by ESA Fly Your Satellite! advisors

Undergraduate Researcher, UBC Radio Science Lab Sept 2024 – Apr 2025
Dynamic Channel Emulator Project CCECE59415.2024.10667238

- Automated RF S-parameter measurements via MATLAB routines controlling VNAs and linear positioning stage, improving repeatability and accuracy for RF data acquisition
- Processed and analyzed RF datasets with pandas library to characterize frequency response, gain uniformity, and measurement variation across test conditions
- Built real-time signal-processing chain with PlutoSDR to receive and retransmit signals with modeled distortions; verified fidelity with spectrum analyzer measurements
- Simulated Doppler shift and free space path loss in MATLAB to emulate realistic orbital pass conditions, supporting system-level verification of RF front-end

Projects

45 nm CMOS Two-Stage Op Amp byuantl.github.io/projects/op-amp

- Optimized two-stage CMOS operational amplifier in 45 nm GPDK using Cadence Virtuoso and Spectre, achieving 52 dB DC gain, 0.65 V output swing, and 48.45 V/μs slew rate under 375 μW power consumption
- Implemented Miller frequency compensation with series RC pole and zero placements stabilizing loop at 618 MHz unity-gain bandwidth with 65° phase margin for high-speed analog operation
- Performed full analog verification including DC, AC, transient, and stability analysis with ADE Assembler

45 nm CMOS 6-Bit SAR ADC byuantl.github.io/projects/sar-adc

- Designed and simulated a 6-bit CMOS successive approximation ADC in 45 nm GPDK achieving 100 MS/s sampling rate and 1 V full-scale input, using Cadence Virtuoso, Spectre, and SPICE simulations
- Developed a custom capacitive DAC and dynamic latch comparator for high-speed mixed-signal conversion
- Implemented SAR control logic in Verilog, verifying bit cycling and timing through SPICE/HDL co-simulation

LeNet-5 CNN Edge AI Acclerator github.com/byuantl/LeNet-5-accelerator

- Deployed hardware-accelerated LeNet-5 CNN on Agilex 3 FPGA using Verilog and Quartus Prime, achieving 4168 FPS throughput (11.9 FPS/MHz) for edge AI inference
- Optimized arithmetic datapath and control logic by quantizing from FP32 to FP11 to fit Agilex 3 resource constraints, reducing utilization to 10.9k ALMs, 14.1k ALUTs, and 31.5k registers