Two-Stage Operational Amplifier

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Contents

Chapter 1

Introduction

Operational Amplifiers (op-amps) are fundamental active devices used by analog designers to amplify an input voltage signal applied to their two input terminals and produce an output voltage signal. Op-amps are used widely for signal conditioning, amplification, filtering and performing mathematical operations in analog circuits. The op-amp is usually characterized by its open-loop gain, bandwidth, stability and power consumption. Op-amps usually have multiple stages to achieve higher voltage gain, sufficient output swing, and improve noise performance.

An ideal Op-Amp exhibits an infinite open-loop gain, infinite input resistance, zero output resistance, infinite bandwidth and zero offset. However, real-world designs must achieve a balance between these trade-offs due to limited supply voltage, technology constraints and power limitations.

This project presents the design and simulation of a two-stage differential to single-ended op-amp based on the given topology in Figure 1.1 implemented in the 45-nm CMOS process. Additionally, the amplifier employs a common-mode feedback (CMFB) circuit to regulate the output common-mode voltage. Miller compensation with a series resistor (R_C) was used for improving the phase margin (PM) and the unity gain frequency (UGF) for stability.

This report will begin with a description of the design objectives, followed by the design process using Cadence EDA tools and the overall performance achieved of the op-amp will be evaluated against key performance metrics.

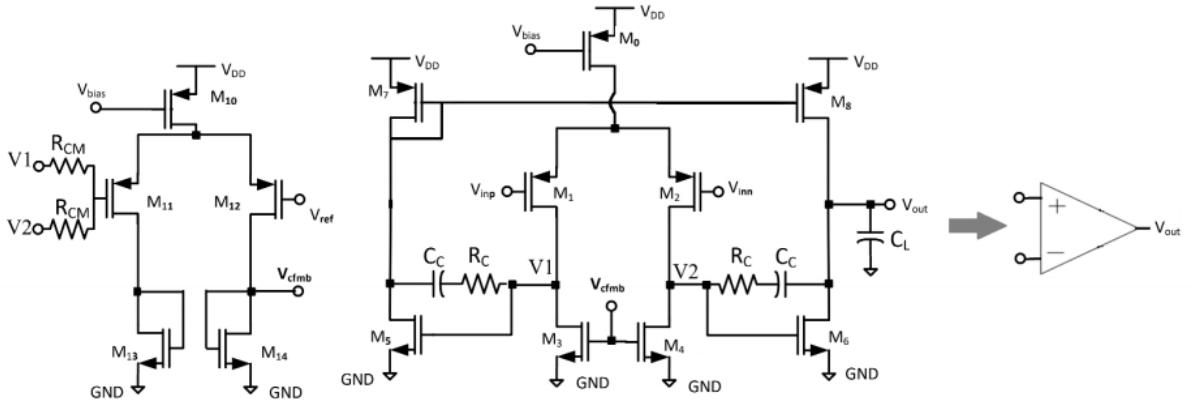


Figure 1.1: Provided op-amp topology

NOTE: V_{inp} & V_{inn} inputs were found to be switched.

Chapter 2

Design Procedure

2.1 Methodology

Firstly, the power budget had to be considered. The CMFB circuit's requirement was $\leq$ 40 µW. Therefore, to calculate the maximum current that can be provided to the CMFB circuit:

$$I_{cmfb} \leq \frac{40\mu W}{1.0V}$$

$$I_{cmfb} \leq 40\mu A$$

Considering the two-stage amplifier circuit where I_1 is the current through stage 1 and I_2 is the current through stage 2:

$$I_{max} = I_1 + I_2$$

$$I_{max} = \frac{40mW}{1.0V} = 400\mu A$$

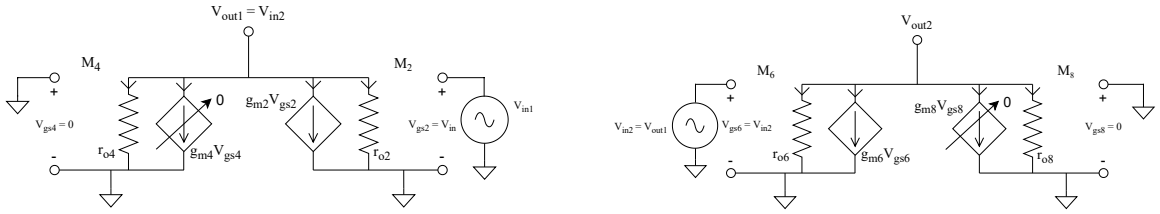
A maximum of 400µA can be distributed to both stages 1 and 2. Initially, it was thought that Stage 1 should be provided with more current than Stage 2, however it was found later into the design process that this made it significantly harder to bias the input stage transistors M_1 and M_2 as well as M_{11} in the CFMB circuit into saturation together. This pushed the design to have more current in Stage 2. The larger current in Stage 2 is beneficial for increasing the transconductance of M_6 which must be at a large enough value to help increase the amplifier's gain.

To ensure the slew rate has been met as it is defined as the maximum rate of output change when the input signal is large:

$$\mathrm{SR} = \frac{\mathrm{I_1}}{\mathrm{C_c}}$$

Initially, C_c was set to 1pF, thus for a minimum slew rate of 20V/µs it must be ensured that I_1 is larger than 20µA.

Moving onto the small signal differential gain, the small signal circuits of stage 1 and stage 2 as seen in figure 2.1 will be analyzed to obtain an expression in terms of transconductance and output resistances of the transistors.



(a) Stage 1 small signal model (b) Stage 2 small signal model

Figure 2.1: Small signal models for the two amplifier stages

Analyzing stage 1:

$$\frac{V_{\text{out1}}}{r_{o4}} + \frac{V_{\text{out1}}}{r_{o2}} + g_{m2}V_{gs2} = 0$$

$$V_{\text{out1}}\left(\frac{1}{r_{o4}} + \frac{1}{r_{o2}}\right) = -g_{m2}V_{\text{in1}}$$

$$\frac{V_{\text{out1}}}{V_{\text{in1}}} = -g_{m2}\left(r_{o4} \parallel r_{o2}\right)$$

Analyzing stage 2:

$$\frac{V_{\text{out2}}}{r_{o6}} + \frac{V_{\text{out2}}}{r_{o8}} + g_{m6}V_{gs6} = 0$$

e

$$V_{\text{out2}}\left(\frac{1}{r_{o6}} + \frac{1}{r_{o8}}\right) = -g_{m6}V_{\text{in2}}$$

$$\frac{V_{\text{out2}}}{V_{\text{in2}}} = -g_{m6}\left(r_{o6} \parallel r_{o8}\right)$$

Calculating the overall amplifier small-signal differential gain:

$$\begin{aligned} A_T &= A_1 \times A_2 \\ &= -g_{m2}\left(r_{o4} \parallel r_{o2}\right) \times -g_{m6}\left(r_{o6} \parallel r_{o8}\right) \end{aligned} \tag{2.1}$$

This leads to equation 2.1 where the overall gain is dependent on the transconductances of transistors M_2 and M_6 as well as the output resistances of M_2, M_4, M_6 and M_8. While simulating in Cadence, it was evident that a larger drain current causes a higher transconductance, but a lower output resistance. This makes sense as recall from the small signal model equations that:

$$r_o = \frac{1}{\lambda I_D} \qquad g_m = \sqrt{2\mu C_{ox}\frac{W}{L}I_D} \qquad I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2(1 + \lambda V_{DS})$$

Before optimizing the gain of the amplifier, Stages 1 and 2 must be biased by selectring an appropriate V_{bias} and V_{ref} necessary for all transistors to operate in the saturation region. This was done by making use of Cadence's Spectre's simulation environment to sweep variables, plot graphs, and check regions of operation of the transistors while satisfying the necessary current requirements for each stage. It was highly important to use the necessary equations required for biasing NMOS and PMOS devices into the saturation region:

$$\begin{aligned} &\text{NMOS:} \quad V_{gs} > V_{th}, \qquad V_{ds} \geq V_{gs} - V_{th} \\ &\text{PMOS:} \quad V_{sg} > |V_{th}|, \qquad V_{sd} \geq V_{sg} - |V_{th}| \end{aligned}$$

For a diode connected MOS: $V_{\text{gs}} \geq V_{\text{th}}$ leads to saturation as $V_{\text{gs}} = V_{\text{ds}}$.

Firstly, stage 1 was loaded onto Cadence and simulations were run to obtain the threshold voltage of the *pmos1v_LVT* and *nmos1v_LVT* transistors. After obtaining $V_{\text{th,n}}$ and $V_{\text{th,p}}$ pertaining to the NMOS and PMOS respectively, the circuit was initially

designed with a V_{ref} and V_{bias} of 0.5 V. Aspect ratios were chosen arbitrarily for the purposes of getting familiar with the circuit.

After stage 1 was biased roughly, stage 2 was added, followed by the CMFB circuit. Following the initial simulations, the aspect ratio of the transistors were tweaked to control the drain currents and come to finalize V_{bias} of 0.46 V and V_{ref} of 0.3 V.

Oftentimes, a common issue was not having a high enough drain-source voltage of the Stage 1 NMOS pair (V_{ds4}) for biasing M_6 into saturation. This was fixed by decreasing the aspect ratio (W/L) to lower the drain current through M_4 which led to a higher V_{ds4}.

Coming back to the stage gain, making use of the simulation environment was highly advantageous as it was possible to sweep variables like W and L to determine the optimal gain while within the maximum current allowed for the respective stage. Specific widths and lengths of the transistors were chosen so that there was a good balance between a small enough g_m that would allow a larger output resistance for each transistor. Ignoring g_{m4} and g_{m8} was possible for the purposes of the small-signal gain, however, making sure that they were still in saturation.

After optimising the gain within power requirements, the circuit in Figure 2.6 was designed. Figure 2.7 shows the schematic on Cadence with the dc-op values annotated. Figure 2.6 displays the transconductances and output resistances of each transistor. To show that the design requirement for gain has been met, the calculation of the theoretical small-signal differential gain using the expression derived before is as follows:

$$\begin{aligned} A_T &= -1.06036 \times 10^{-3} \left(28.5872\text{k} \parallel 31.3777\text{k}\right) \times -1.59238 \times 10^{-3} (28.5872\text{k} \parallel 31.3777\text{k}) \\ &= 377.8255 \text{ V/V} = 51.55 \text{ dB} \end{aligned}$$

At this point, the total current consumed by the CMFB circuit is 40.3535 µA while the amplifier consumes a total of 375.293 µA. Both values fall within the given design constraints.

Now, the open-loop transfer function will be examined to ensure that low-frequency gain, PM, and UGF targets are met. With $R_c = 0\ \Omega$ and $C_c = 1$ pF, the UGF and PM were too low at approximately 155 MHz, and 11° respectively. Keeping the miller capacitor at 1 pF and increasing R_c to 1M lead to an increase in the UGF to 955 MHz, however PM remained relatively unchanged. At this point, while the UGF requirement is met, the PM will still need to increase. Instead, if R_c is kept at 0 and C_c is increased from 1 pF to 10 pF, it was evident that this decreases the UGF, to 35.68 Mhz, but increases the PM to 27°. Following these observations, it would also be useful to test the effect of changing the width of the Stage 2 MOS devices as the zero being placed depends on the transconductance of the Stage 2 MOS devices. We can test this be sweeping both the multipliers of the top PMOS and bottom NMOS in Stage 2. This yielded figures 2.2 and 2.3, where it was realised that increasing the width of the bottom NMOS device increases the PM. On the other hand, increasing the top PMOS device provided minimal change in UGF or PM.

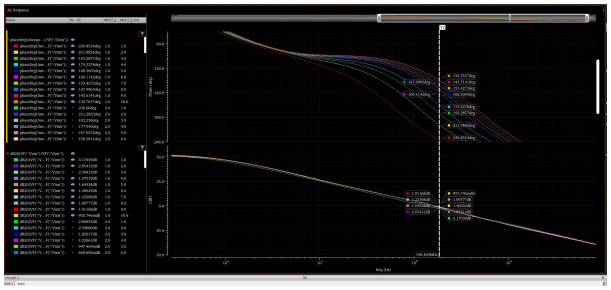


Figure 2.2: Effect of increasing the stage 2 nmos multiplier on PM and UGF

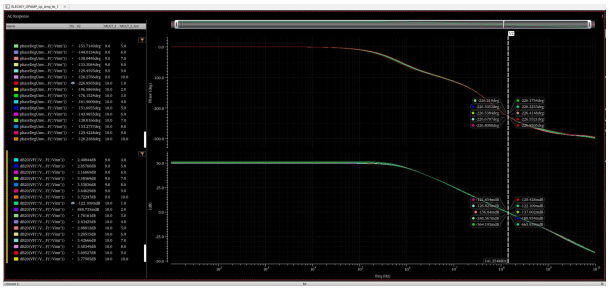


Figure 2.3: Effect of increasing the stage 2 pmos multiplier on PM and UGF

In order to minimise changes to the circuit, it was first attempted to achieve the PM and UGF using solely the compensation capacitor and resistor. Thus sweeping the capacitor and resistor lended the following graph that was used to recognise that a smaller resistor seemed better to improve the PM while maintaining a high enough UGF to meet the design requirement. A small capacitor also helps with having minimal decerase in the bandwidth as seen in figure 2.5.

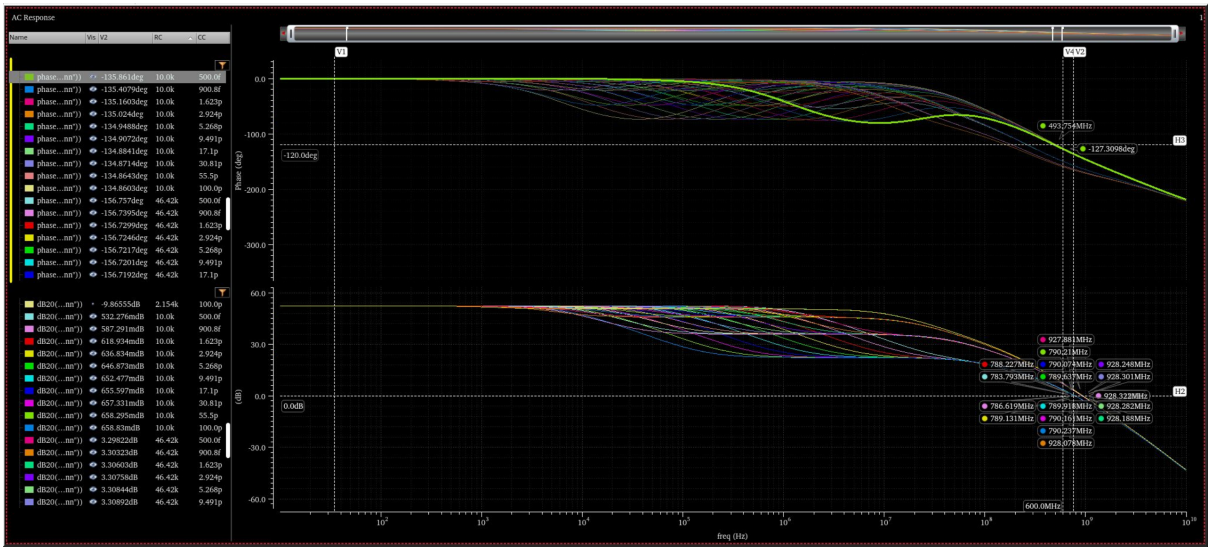


Figure 2.4: Effect of varying R_c and C_c

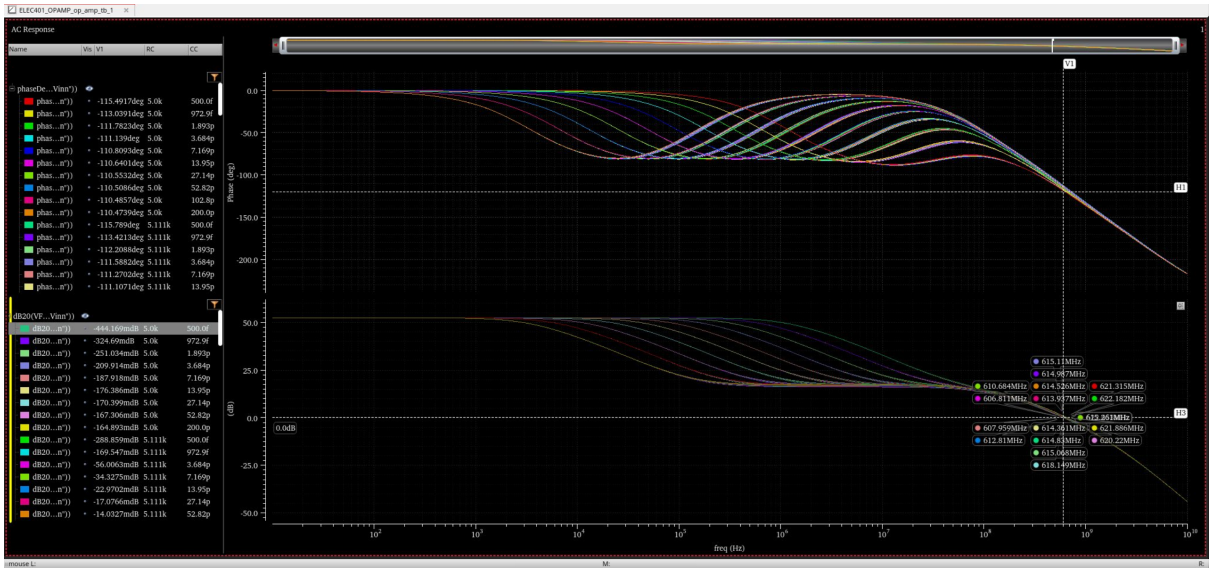


Figure 2.5: Effect of higher C_c on reducing bandwidth while R_c kept constant

Finally, running further simulations, to narrow down values, a compensation resistor and capacitor value of 5.44 k and 1.90 p were selected to nail the design requirements down to a UGF of 618 MHz and PM of 65.38°(refer to section 3.2). Now, calculating the slew rate to ensure it is greater than 20 V/µs:

$$\begin{aligned} \text{SR} &= \frac{92.055\mu\text{A}}{1.90\text{pF}} \\ &= 48.45\text{V}/\mu\text{s} \end{aligned}$$

Something that should have been considered earlier in the design process is the differential output swing of the amplifier, as meeting this target requires resizing the second stage. To find the upper and lower bounds of the output voltage:

Consider M8:

$$\begin{aligned} V_{sd8} &\geq V_{sg8} - |V_{th8}| \\ V_{d8} &\leq V_{g8} + |V_{th8}| \\ V_{d8} &\leq 445.986\text{ mV} + |-324.189\text{ mV}| \\ V_{d8} &\leq 770.175\text{ mV} \end{aligned}$$

Consider M6:

$$\begin{aligned} V_{ds6} &\geq V_{gs6} - |V_{th6}| \\ V_{d8} &\geq 491.633\text{ mV} - |368.171\text{ mV}| \\ V_{d8} &\geq 123.462\text{ mV} \end{aligned}$$

This effectively lends an output voltage swing of 647 mV. In order to meet the requirement of an output swing ≥ 0.75 V, it would be possible to increase the upper bound by increasing the gate voltage of the PMOS in the second stage. This would require increasing the drain-source voltage of the second-stage NMOS by decreasing W/L to drop the current through stage 2. This would sacrifice some gain due to a decrease in transconductance, however as the output resistance increases, this loss in gain should be minimal.

2.2 Design Schematic

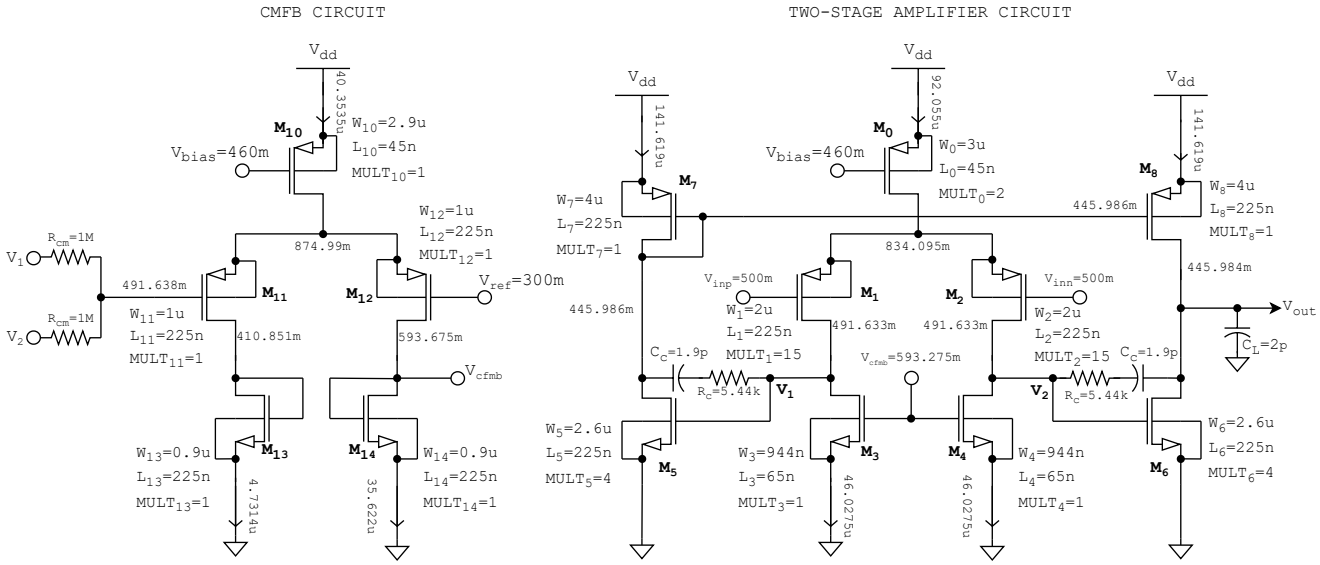


Figure 2.6: Diagram of component parameters

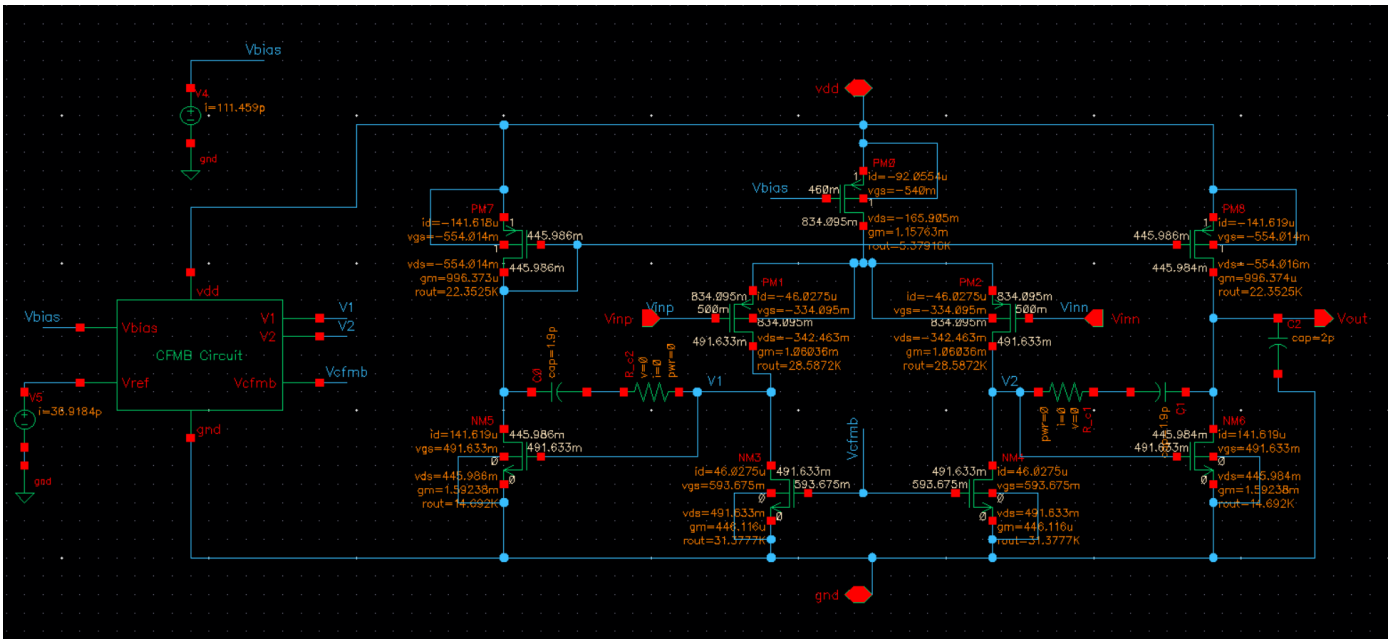


Figure 2.7: Amplifier circuit dc-op with MOS output resistance annotated

2.3 Overall Performance

Most design requirements have been met as noted in the table below. Two areas where the design fell short were in the differential output swing (by 103 mV) and the output DC level (by 54 mV).

Increasing the differential output swing can be done by increasing the gate voltage of the second-stage PMOS as mentioned before. To increase the output DC level, the CMFB circuit will have to be adjusted through V_{ref} or the aspect ratios of the transistors to shift the output CM level upward while maintaining saturation.

Specification	**Requirement**	**Achieved**
V_{DD}	1.0 V	1.0 V
GND	0 V	0 V
C_L	2 pF	2 pF
Nominal input common-mode (input DC level)	$V_{DD}/2$=0.5 V	0.5 V
Nominal output common-mode (output DC level)	$V_{DD}/2$=0.5 V	0.446 V
Two-stage power consumption	$\leq$ 0.4 mW	0.375 mW
CMFB circuit power	$\leq$ 40 µW	40.35 µW
Differential output Swing	$\geq$ 0.75 V	0.65 V
Low-frequency differential gain	$\geq$ 46 dB	52.44 dB
Small-signal unity gain frequency	$\geq$ 600 MHz	618 MHz
Phase Margin	$\geq 60^\circ$ & $\leq 90^\circ$	65.39°
Slew Rate	$\geq$ 20 V/µs	48.45 V/µs
Maximum length of transistors (L_{min}=45 nm)	5×L_{min}=225 nm	225 nm
Maximum width per Multiplier	4 µm	4 µm
Maximum Multiplier of transistors	50	15

2.4 CMFB Architecture

The CMFB circuit provides a feedback loop that controls and stabilises the output common-mode (CM) voltage of the amplifier. If the gate of M_{11} is equal to the reference voltage, current is divided equally through the CMFB circuit. However, if the output CM is too high (greater than V_{ref}), the CMFB circuit will pull it back down as the source to gate voltage of M_{11} drops, thereby decreasing the current through the branch and dropping V_{cfmb}. This drop in V_{cfmb} will decrease the current going through stage 1, and so increasing the CM differential output voltage of the amplifier. The opposite happens when the output CM is lower than V_{ref}. V_{ref} is not necessarily the output common mode voltage desired (0.5 V), rather it is an internal reference for the CMFB circuit due to the design choices.

Chapter 3

Performance Results

3.1 DC-OP Point

A DC op-point simulation was performed with a 0.5V common-mode input. All transistors were confirmed to operate in saturation(region 2) as seen in Figures 3.1 and 3.2.

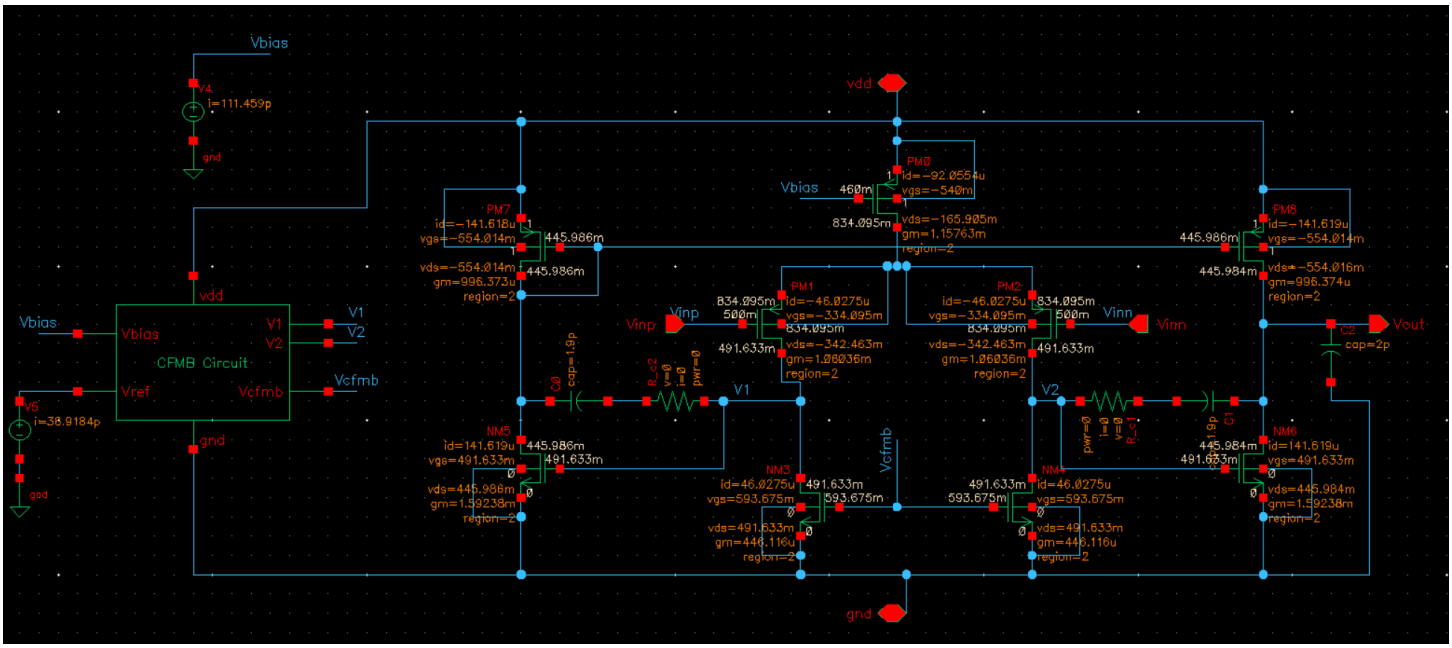


Figure 3.1: Amplifier Circuit DC-OP With Regions Annotated

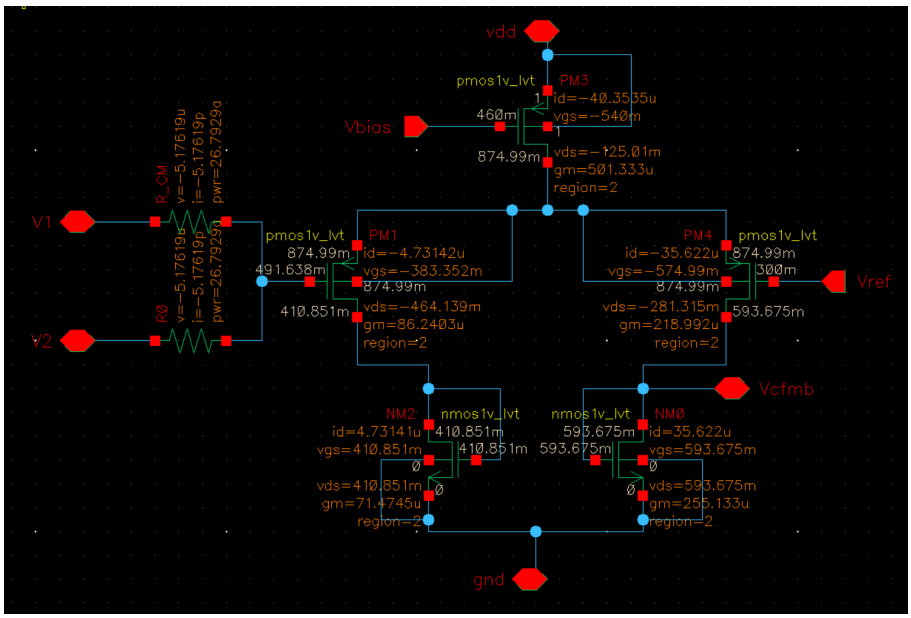


Figure 3.2: CMFB Circuit DC-OP With Regions Annotated

3.2 Open-Loop Transfer Function

The following bode plot was obtained with a differential small-signal AC input:

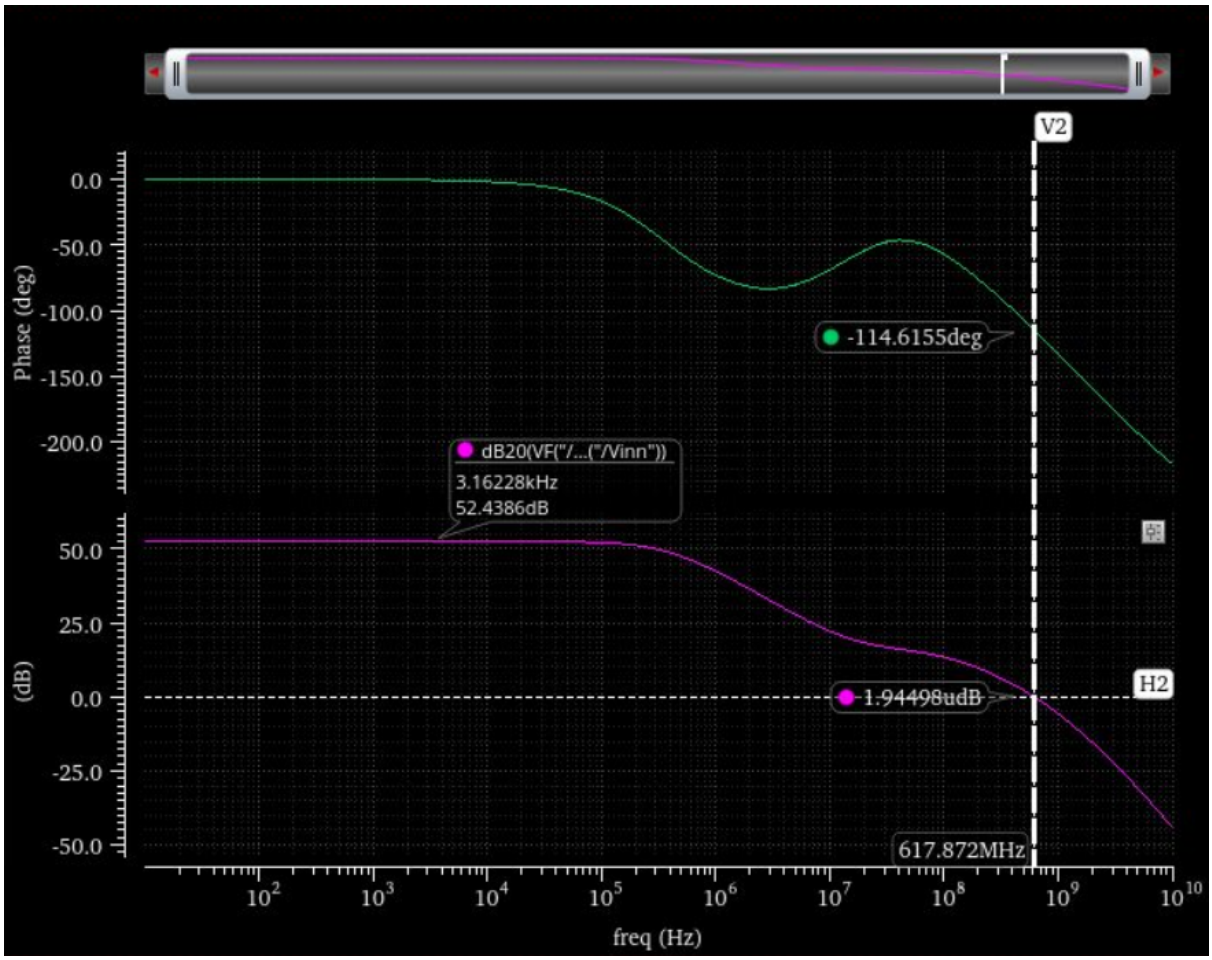


Figure 3.3: Open-loop transfer function

3.2.1 Phase Margin

The phase margin is the difference between the phase at UGF and -180°. PM is a crucial factor as it indicates the circuit's stability by showing the extra phase shift required in order for the circuit to become unstable. A high PM, while is more stable, slows down the time response of the system. As seen in Figure 3.3:

$$\text{PM} = 180° - 114.6155° = 65.3845°$$

This meets our design requirement of $\geq 60°$ & $\leq 90°$.
The plot also shows that a UGF of 617.872 MHz was achieved, which meets the design requirement of ≥ 600 MHz.

3.2.2 Low-Frequency Gain

As annotated in Figure 3.3, the low frequency gain is approximately 52.44 dB.

3.3 Closed-Loop Transfer Function

The following circuit in Figure 3.4 was used to create a bode plot of the closed-loop system and find the 3-dB frequency. Vin1 is an AC source with an Amplitude of 1 u. Figure 3.5 is produced which presents the closed-loop AC gain of 10.65 mdB. The resulting 3-dB frequency of the system is 390.90 MHz where -2.989 dB lies.

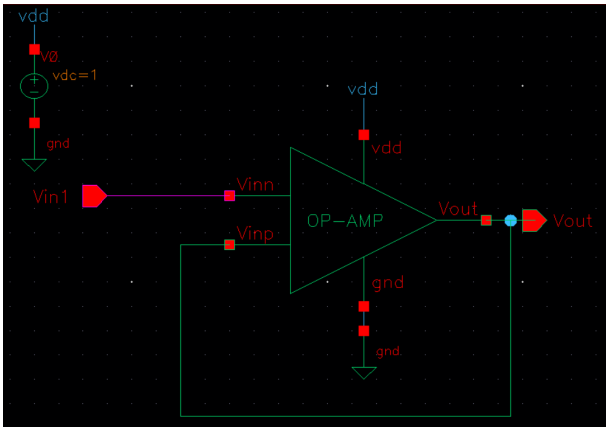


Figure 3.4: Designed op-amp in unity buffer configuration

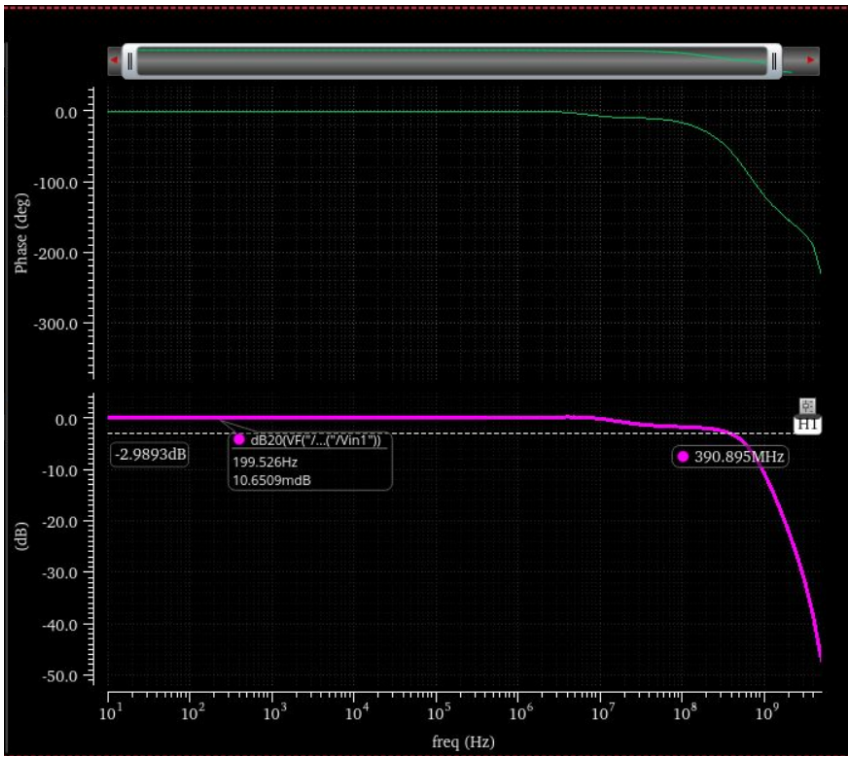
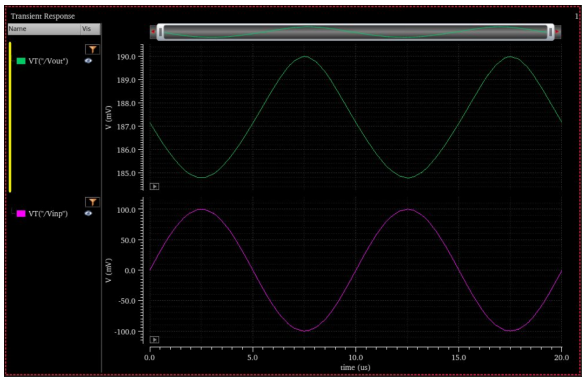


Figure 3.5: Closed-loop Transfer Function with 3-dB frequency annotated

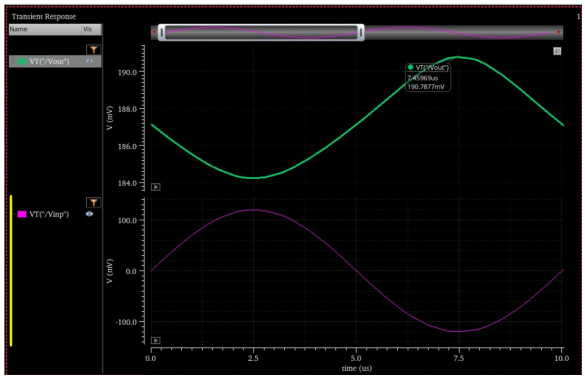
3.4 Maximum Undistorted Output Swing

Firstly, a 0.1 MHz differential sinusoidal input is applied to the open-loop circuit with an appropriately small amplitude that avoids distortion at the input. The amplitude is then gradually increased until distortion occurs. Using the simulation environment, an amplitude sweep was run to look at the approximate voltage where distortion occurs. As seen in Figure 3.6(d), distortion starts to appear as the peak of the waveform gets chopped

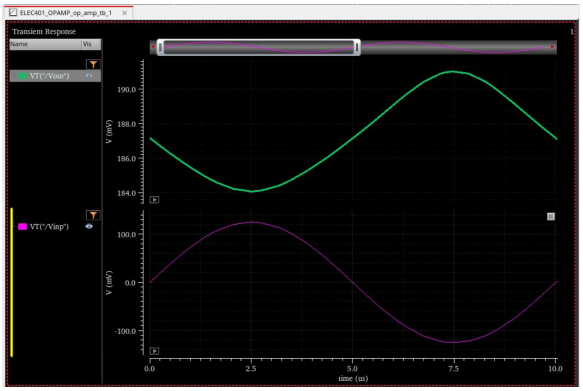
off. Thus, the maximum undistorted output swing was found to be approximately 125 mV.



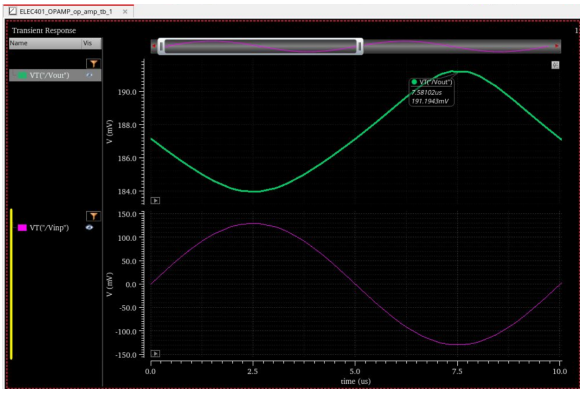
(a) 100 mV



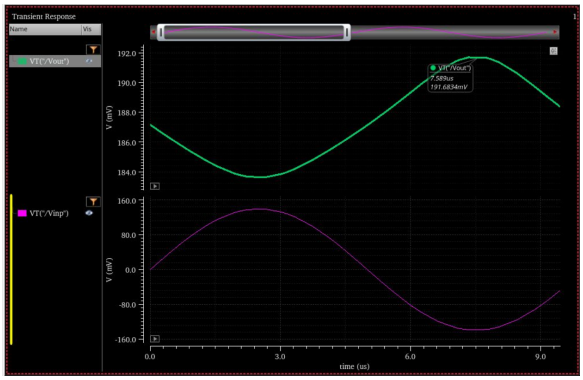
(b) 120 mV



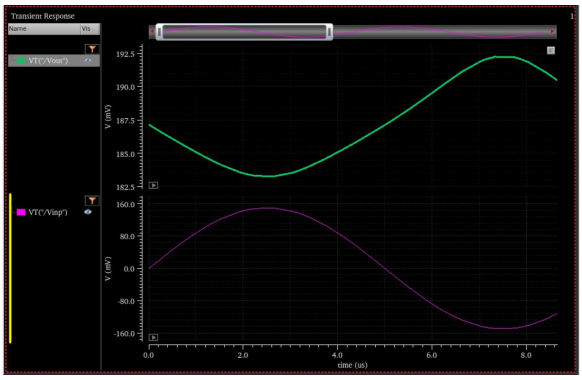
(c) 125 mV



(d) 130 mV



(e) 140 mV



(f) 150 mV

Figure 3.6: Transient waveforms of 0.1 MHz differential sinusoidal input

3.5 Transient Responses: Settling Behaviour & Slew rate

To plot the transient response of the step functions, the op-amp is connected as in Figure 3.7. To calculate the small-signal 10 to 90% settling time, the difference between the final settling value of the output voltage waveform and the input voltage waveform is first found. After finding the difference, $0.9\times\Delta V$ or $0.1\times\Delta V$ is added to get the 90% or 10% voltage values, respectively. The large-signal initial rising/falling slopes can be calculated by the rise/run of the initial linear region.

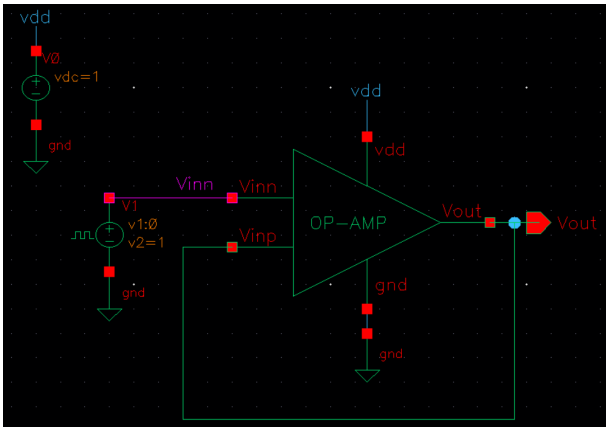


Figure 3.7: Step-response circuit configuration

3.5.1 0.495 V - 0.505 V

Calculating the 10 to 90% settling time as seen in Figure 3.9:

$$106.0863\text{ ns} - 100.4288\text{ ns} = 5.6575\text{ ns}$$

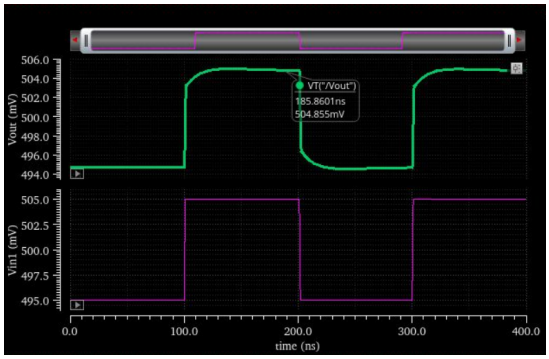


Figure 3.8: Closed-loop step response (495 mV–505 mV)

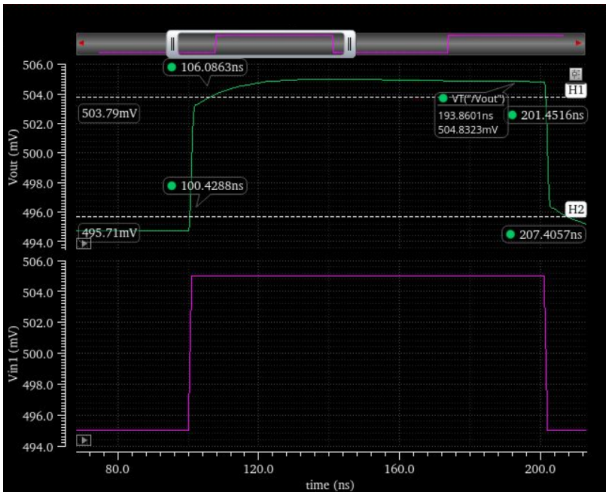


Figure 3.9: Annotated 10-90% time (495 mV–505 mV)

3.5.2 0.505 V - 0.495 V

Calculating the 10 to 90% settling time as seen in Figure 3.11:

$$106.8429\text{ ns} - 100.4577\text{ ns} = 6.3852\text{ ns}$$

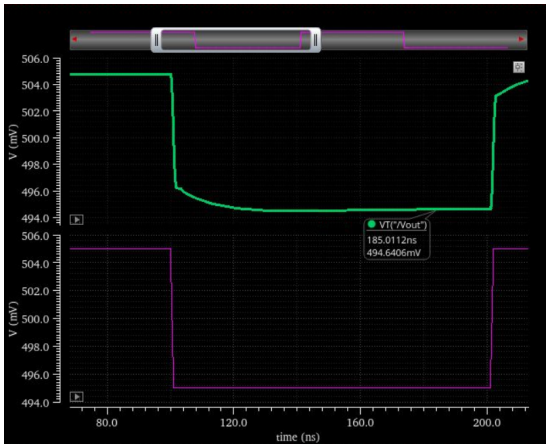


Figure 3.10: Closed-loop step response (505 mV–495 mV)

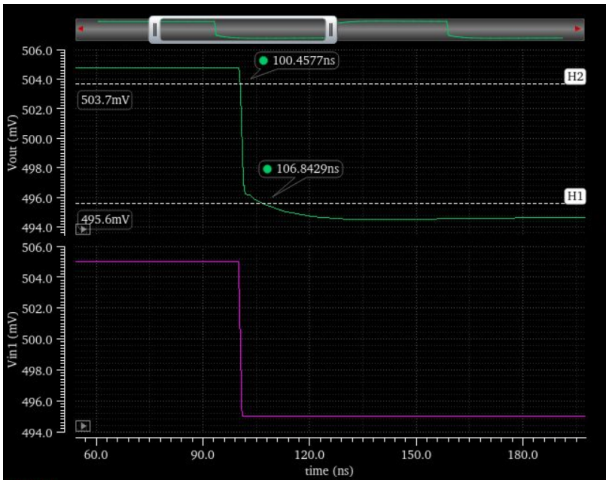


Figure 3.11: Annotated 10-90% time (505 mV–495 mV)

3.5.3 0 V - 1 V

Calculating the initial rising slope of the output as seen in Figure 3.13:

$$\text{SR} = \frac{285.249\ \text{mV} - 208.8412\ \text{mV}}{101.2472\ \text{ns} - 100.8223\ \text{ns}} = 179.8\ \text{mV/ns} = 179.8\ \text{V/µs}$$

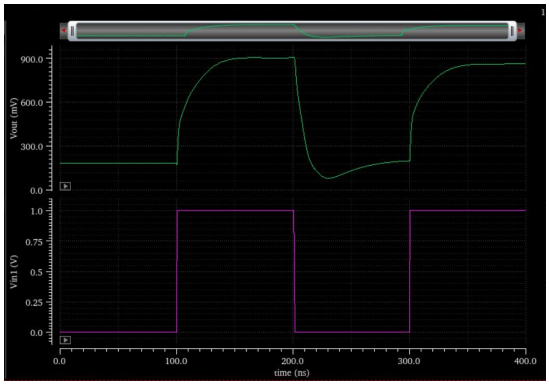


Figure 3.12: Closed-loop step response (0–1 V)

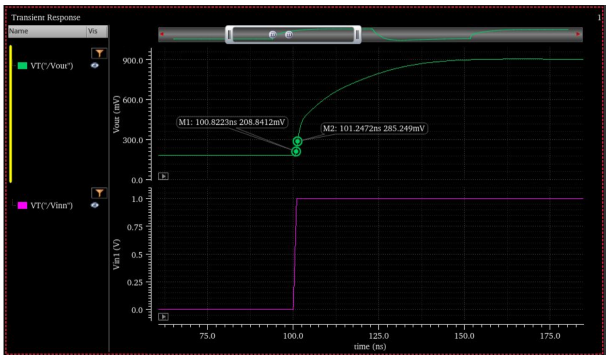


Figure 3.13: Annotated initial rising slope (0–1 V)

3.5.4 1 V - 0 V

Calculating the initial falling slope of the output as seen in Figure 3.13:

$$SR = \frac{759.0422\ \text{mV} - 814.2533\ \text{mV}}{102.0432\ \text{ns} - 101.4839\ \text{ns}} = -98.715\ \text{mV/ns} = -98.715\ \text{V/µs}$$

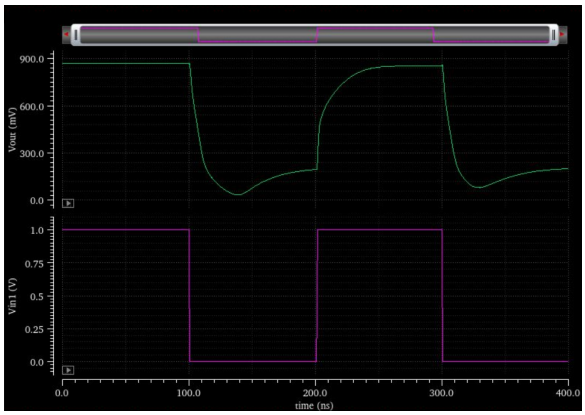


Figure 3.14: Closed-loop step response (1–0 V)

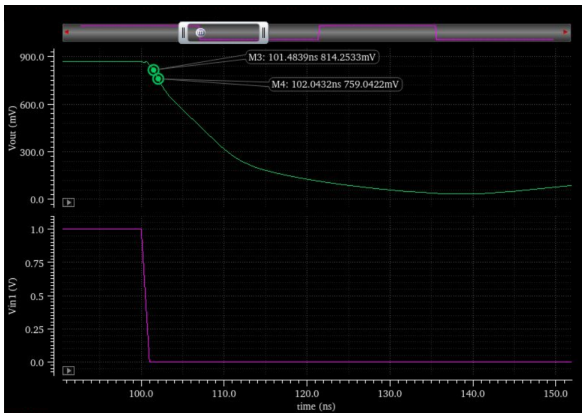


Figure 3.15: Annotated initial falling slope (1–0 V)

Chapter 4

Conclusion

The design and simulation of a two-stage CMOS operational amplifier was completed using the 45-nm process and a 1 V supply. The amplifier meets most of the specified design requirements, however, two specifications that were not fully satisfied were namely the nominal output CM voltage and the differential output swing. The nominal output CM voltage fell short by 54 mV at 446 mV rather than 500 mV. Meanwhile, the differential output swing fell short by 103 mV at 0.647 V compared to the requirement of $\geq$0.75 V.

In order to improve on the design, increasing the upper bound of the output voltage limit can be done by increasing the gate voltage of the second-stage PMOS device. This would require increasing the drain-source voltage of the second-stage NMOS by decreasing W/L to drop the current through Stage 2. As a result, transconductance will drop, but output resistance will increase, hence the loss in gain within stage 2 should be minimal.

To improve the output DC level, adjustments to the CMFB circuit will have to be made through the sizing and reference voltage.

Overall, this project provided valuable insights into the practical challenges of designing analog CMOS circuits. Through designing with EDA tools such as Cadence, it was highly advantageous to run 100 parameter simulations to examine the effects of changing parameters and optimising the design. The experience gained through this design process will be directly applicable to more advanced analog and mixed-signal IC designs.