Design, Analysis and Simulation of a CMOS Low Noise Amplifier

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***Abstract*—This paper presents the design, analysis, and simulation of a fully-integrated CMOS Low Noise Amplifier (LNA) operating at a center frequency of 5.25 GHz. The LNA is designed using 45nm PDK models with a supply voltage of 1.0V. The amplifier achieves a gain ($|S_{21}|$) greater than 15 dB, input and output matching ($|S_{11}|$ and $|S_{22}|$) below -10 dB, reverse isolation ($|S_{12}|$) less than -30 dB, and noise figure below 2.2 dB across the frequency range of interest. The design methodology, hand calculations, simulation results, and optimization techniques for power consumption are discussed in detail.**

***Index Terms*—CMOS, input matching, low noise amplifier (LNA), noise figure, S-parameters, 45nm technology.**

I. Introduction

THIS project focuses on the design of a fully-integrated CMOS LNA using 45nm technology with a center frequency of 5.25 GHz. The design must meet stringent specifications including gain greater than 15 dB, input and output return loss better than -10 dB, reverse isolation better than -30 dB, noise figure below 2.2 dB, and IIP3 greater than -7 dBm, all while minimizing power consumption with a 1.0V supply.

This paper is organized as follows: Section II presents the achieved specifications and simulation results. Section III describes the design methodology and hand calculations. Section IV covers power consumption optimization. Section V concludes the paper.

II. Achieved Specifications and Simulation Results

A. Achieved Specifications

TABLE 1
Required Specifications and Achieved Results

Specification	**Requirement**	**Achieved Result**
Vdd	1.0 V	1.0 V
Center Frequency, f_c	5.25 GHz	5.25 GHz
Bandwidth, BW	200 MHz	200 MHz
| S11 | @ f_c and +/-100MHz	< -10 dB	< -10.14 dB
| S22 | @ f_c and +/-100MHz	< -10 dB	< -10.03 dB
| S12 | @ f_c and +/-100MHz	< -30 dB	< -41.9 dB
| S21 | @ f_c and +/-100MHz	> 15 dB	> 15.0 dB
Noise Figure, NF @ f_c and +/-100MHz	< 2.2 dB	< 2.063 dB
IIP3	> -7 dBm	-6.967 dBm
Load capacitance (from next stage)	50 fF	50 fF
Power Consumption	< 5 mW	2.862 mW

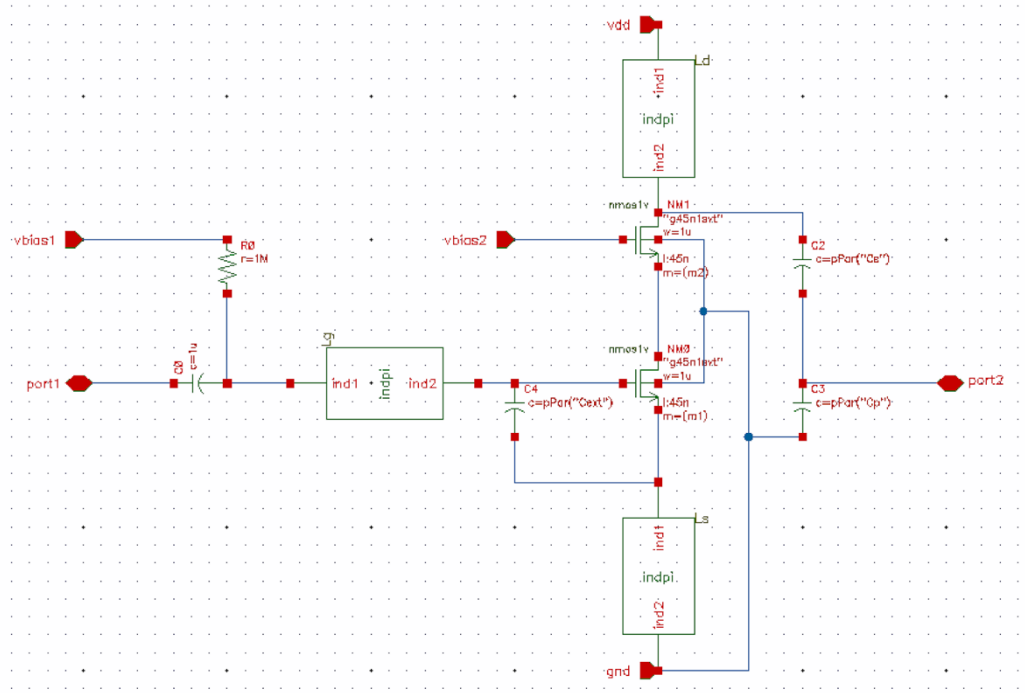


Fig 1. Low Noise Amplifier Schematic

The LNA was simulated using Cadence Spectre RF with 45nm PDK models with the following testbench. S-parameter analyses were performed from 1 GHz to 10 GHz to evaluate matching and gain. Periodic steady-state (PSS) and periodic AC (PAC) analyses were used for IIP3 simulation with two tones at 5.25 GHz and 5.251 GHz (1 MHz separation).

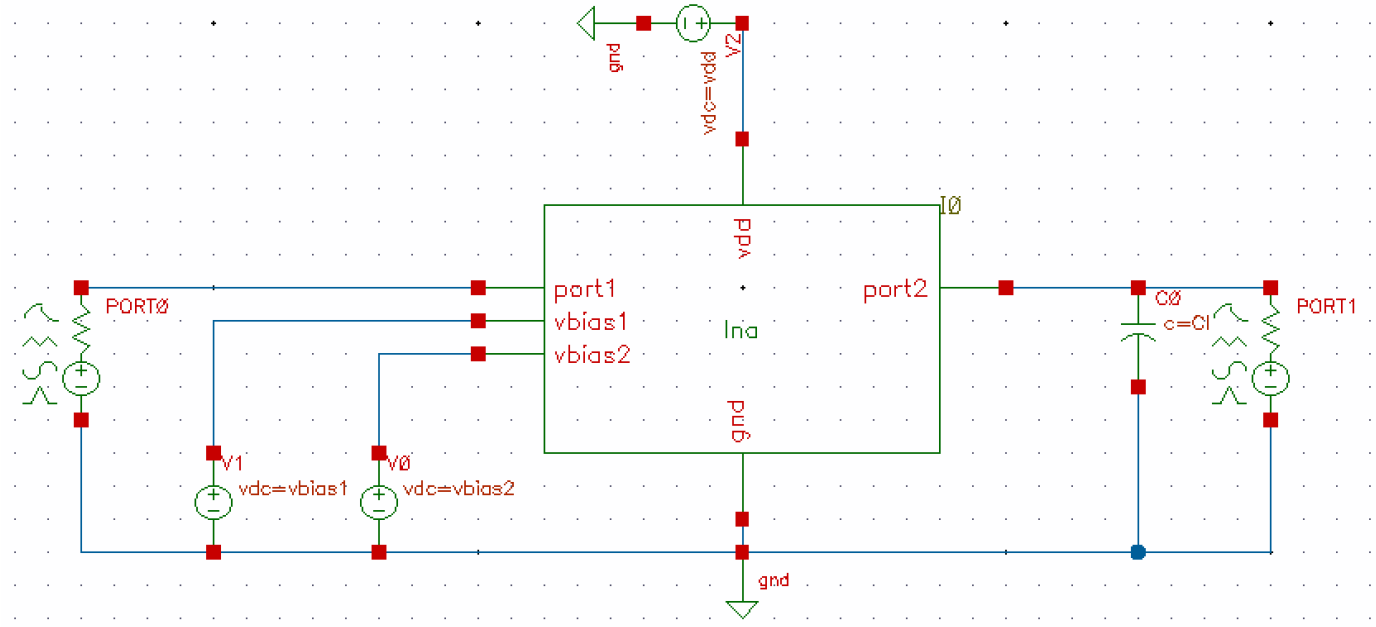
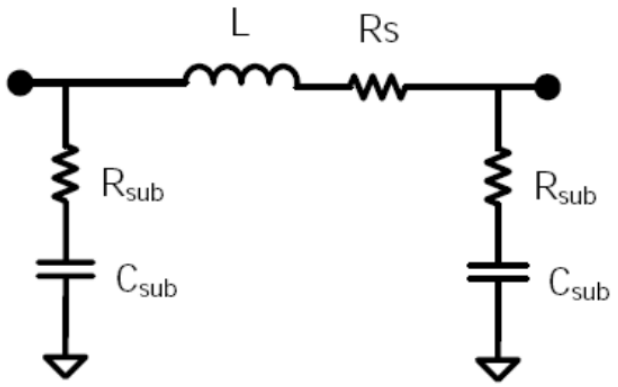


Fig 2. LNA Testbench

B. DC Operating Points

A Pi model inductor was used for the design of this LNA.



$$Rs = -0.02\left(\frac{L}{1nH}\right)^2 + \left(\frac{L}{1nH}\right) + 1.5$$

$$Rsub = 0.0789\left(\frac{L}{1nH}\right) + 3.4893\left(\frac{L}{1nH}\right)^{-1} + 31.707$$

$$Csub\ (in\ pF) = -0.0005\left(\frac{L}{1nH}\right)^2 + 0.0312\left(\frac{L}{1nH}\right) + 0.0543$$

Fig 3. Pi Model Inductor

The following DC operating point values were used for the components of the LNA.

TABLE 2
DC Operating Points of LNA Components

Vdd	1.0 V
Vbias1	0.65 V
Vbias2	1.0 V
C0	1 uF
R0	1 MΩ
Cext	125 fF
Cp	1.19 pF
Cs	395 fF
Ld	1.89 nH
Lg	2.85 nH
Ls	0.34 nH
NM0 gm	34.9563 mS
NM0 W/L	125*(1u/45n)
NM0 Vds	328.849 mV
NM0 Vdsat	95.1356 mV
NM1 gm	36.0671 mS
NM1 W/L	120*(1u/45n)
NM1 Vds	656.393 mV
NM1 Vdsat	88.2819 mV

C. S-Parameter Results

The S-parameters of the LNA were measured with 50 Ω input and output impedance and a 50 fF capacitive load at the output. A zoomed in figure indicating the required bandwith around 5.25 GHz is provided. Precise values at the edges were measured as reported in TABLE 1 and the specifications were thus met.

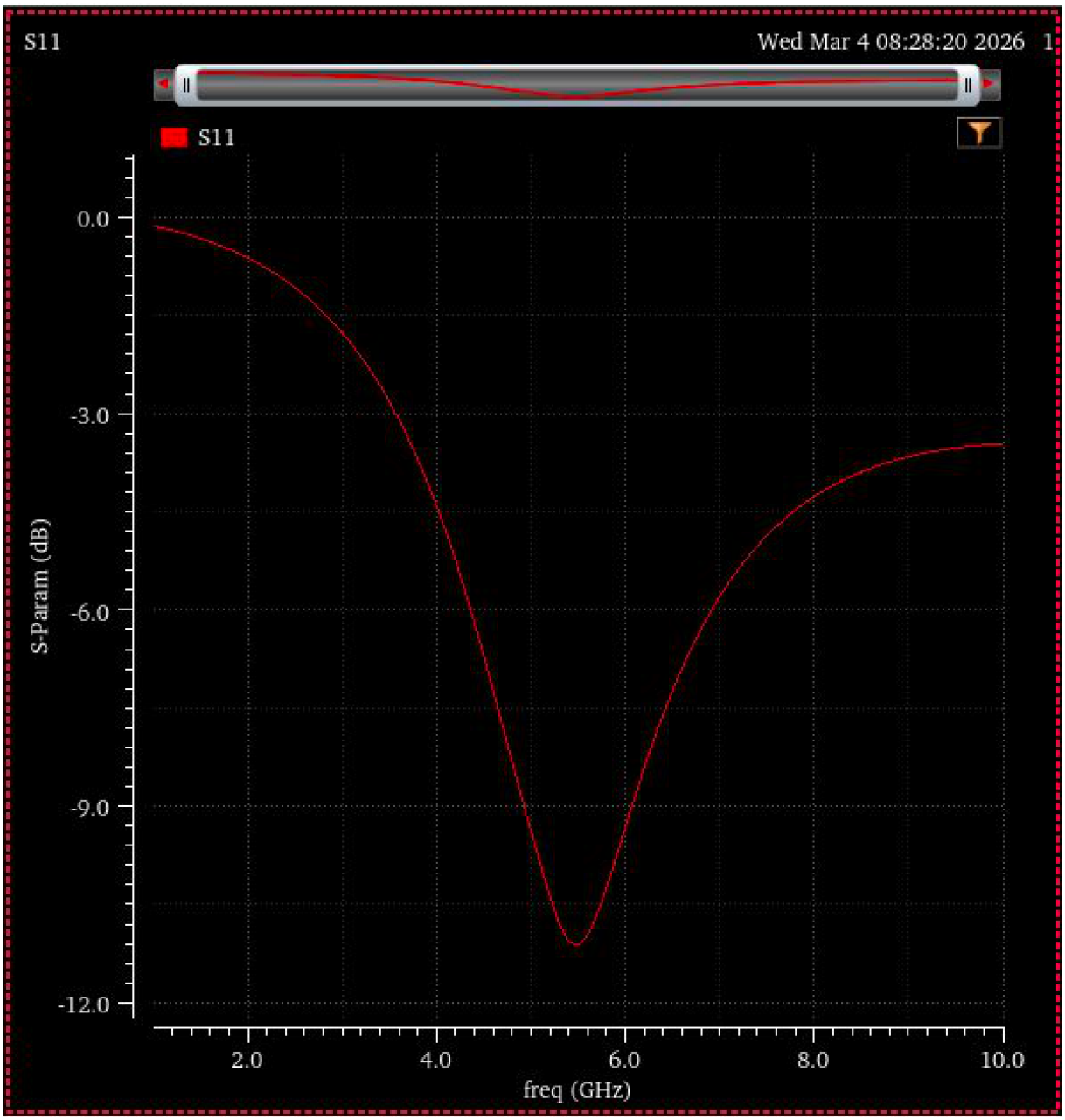


Fig 4. S11 Parameters

Figure 4 shows the input return loss ($|S_{11}|$) versus frequency. At 5.25 GHz, $|S_{11}|$ = -10.6 dB, meeting the specification of < -10 dB. Across the ±100 MHz bandwidth, $|S_{11}|$ remains below -10.14 dB, indicating good input matching.

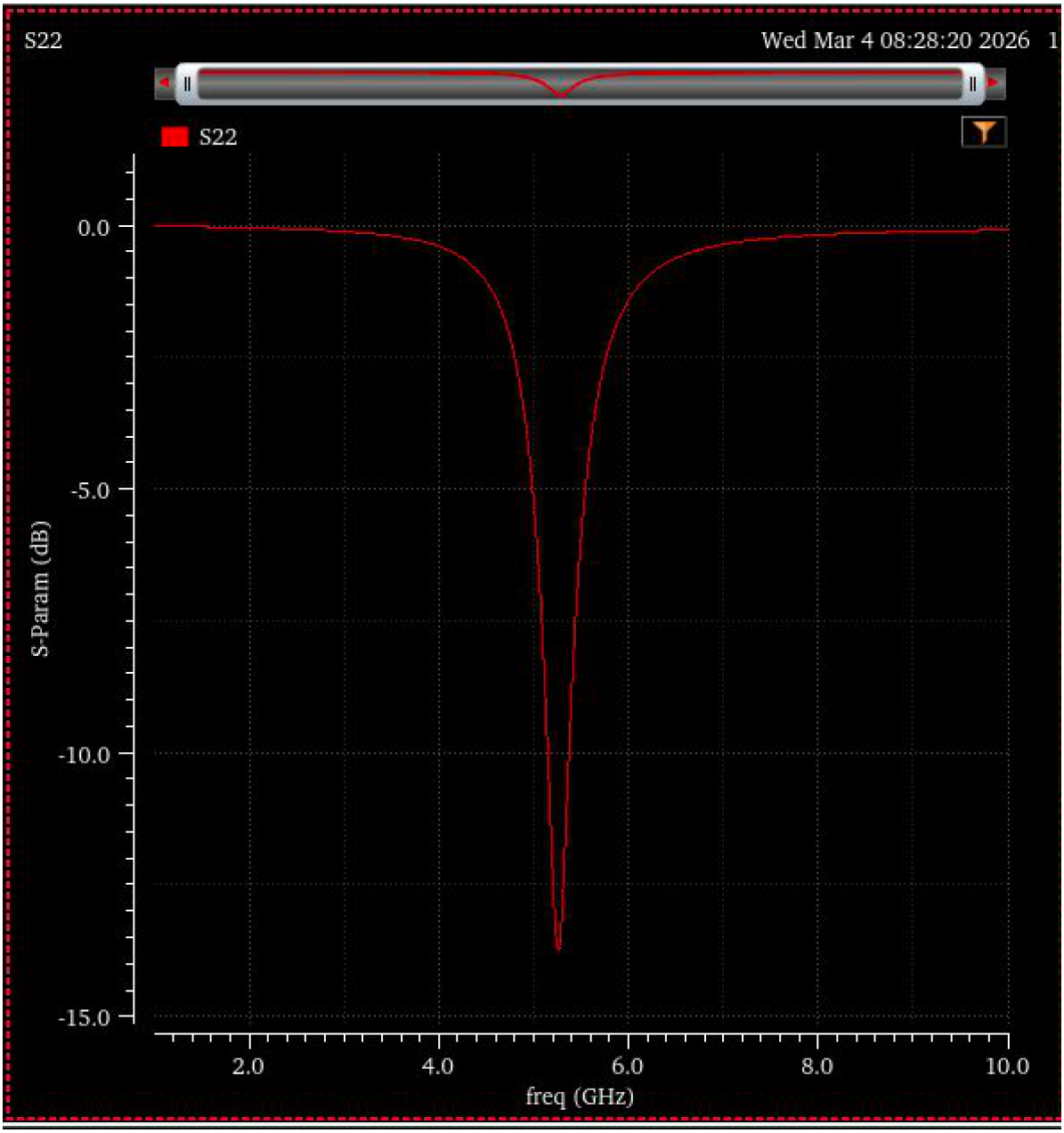


Fig 5. S22 Parameters

Figure 5 displays the output return loss ($|S_{22}|$). At 5.25 GHz, $|S_{22}|$ = -13.7 dB, meeting the -10 dB specification. The output matching remains better than -10.03 dB across the bandwidth.

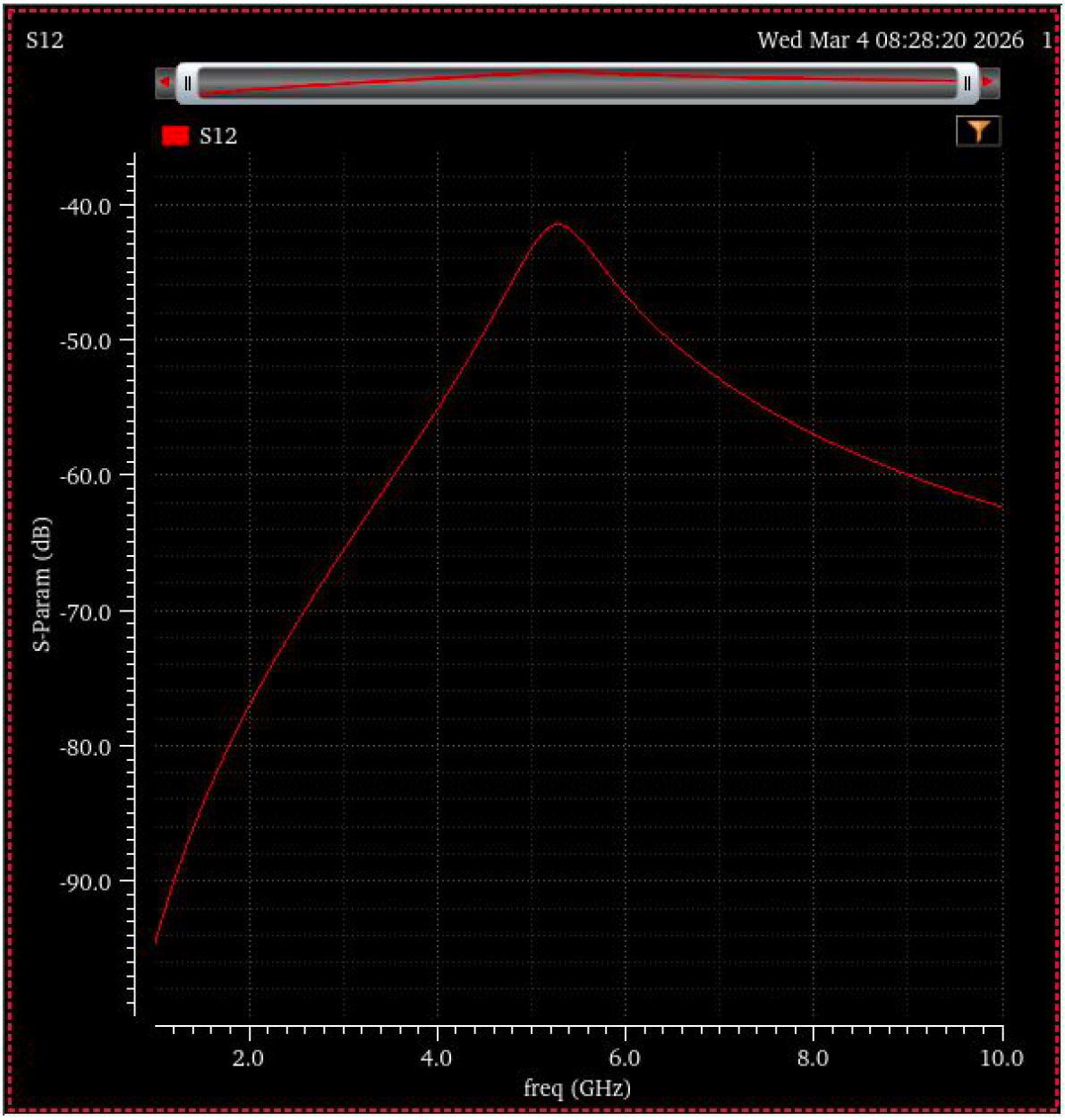


Fig 6. S12 Parameters

Figure 6 shows reverse isolation ($|S_{12}|$). At 5.25 GHz, $|S_{12}|$ = -41.52 dB, well below the -30 dB requirement, confirming good isolation provided by the cascode configuration. The reverse transmission remains better than -41.5 dB across the bandwidth.

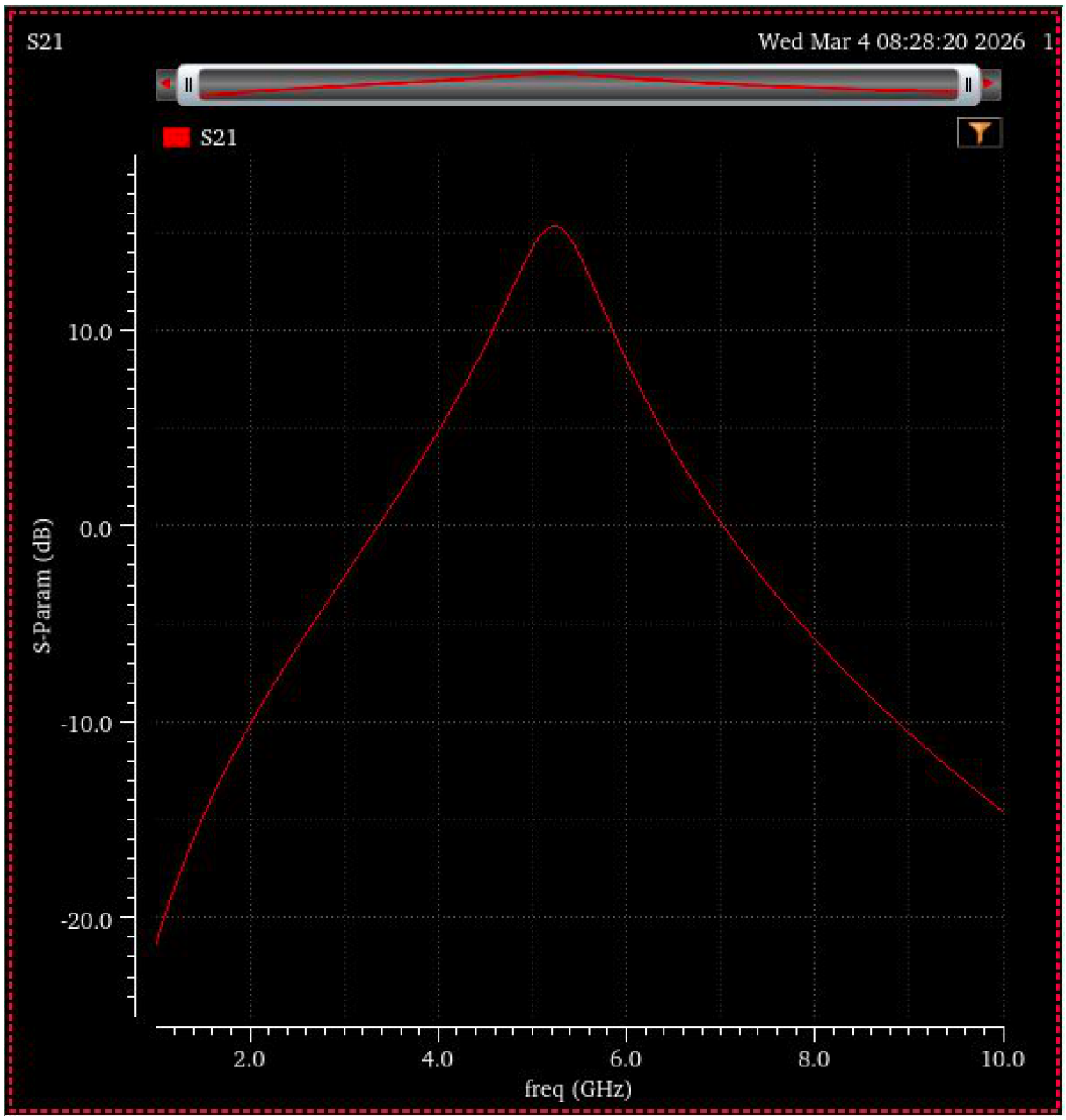


Fig 7. S21 Parameters

Figure 3 presents the gain ($|S_{21}|$) performance. The peak gain at 5.25 GHz is 15.3 dB, exceeding the 15 dB requirement. The forward transmission remains better than 15.0 dB across the bandwidth.

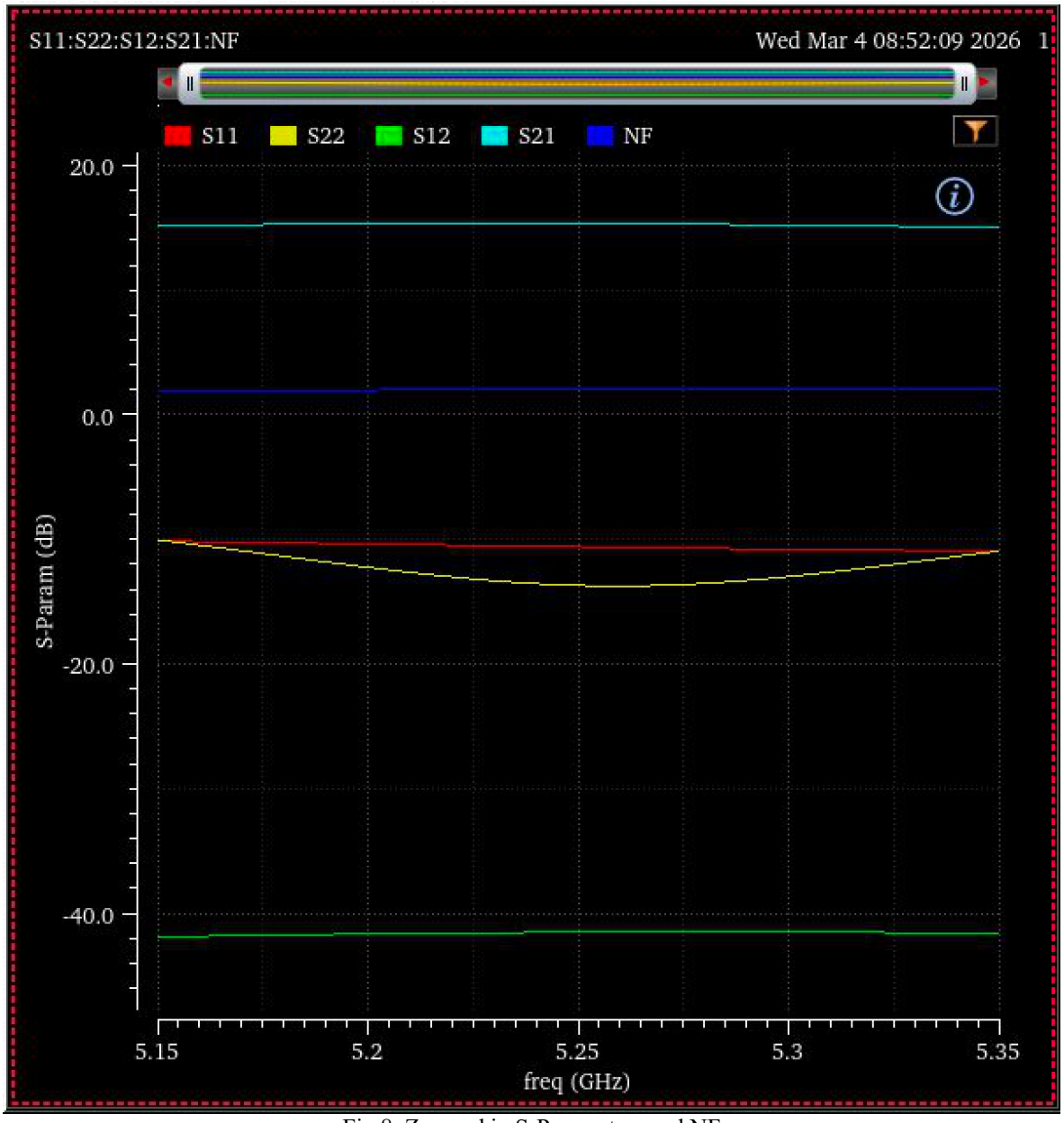


Fig 8. Zoomed in S-Parameters and NF

Figure 8 shows a zoomed in graph of the S-parameters for better viewing.

D. Noise Figure Performance

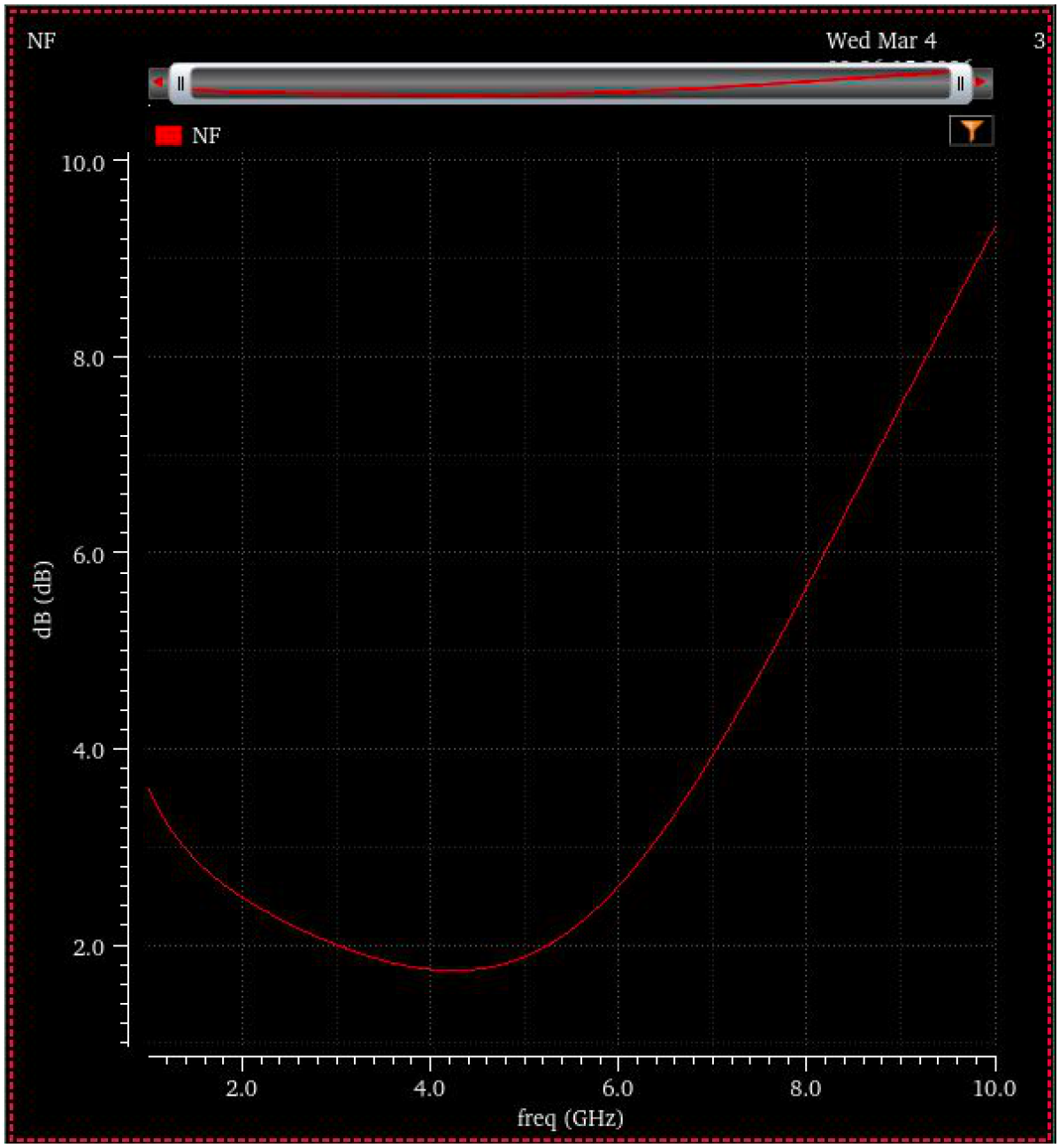


Fig 9 Noise Figure vs. Frequency

Figure 9 illustrates the noise figure versus frequency. At 5.25 GHz, NF = 2.003 dB, satisfying the < 2.2 dB requirement. Across the ±100 MHz bandwidth, NF remains below 2.063 dB. From the Noise Figure Summary, Lg had the largest effect on noise, followed by the transistor NM0, therefore we focused on optimizing Lg to reduce the NF.

E. Linearity Performance

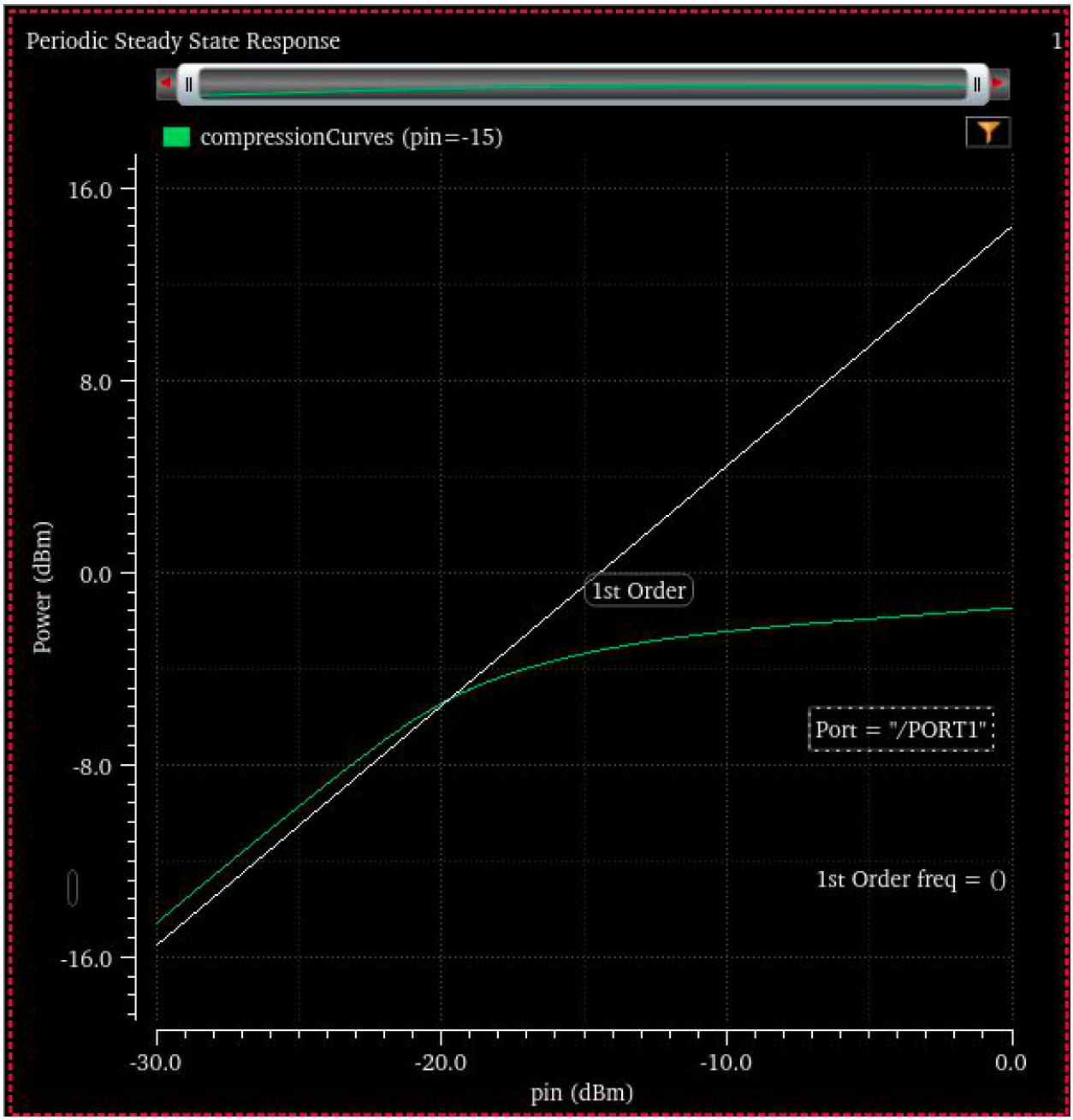


Fig 10. 1 dB Compression Point

Figure 10 shows an initial measurement of the 1 dB compression point as an initial starting point for linearity measurements. The 1 dB compression point was found to be around -20 dBm so for IIP3 measurements, we should extrapolate around ~ -40 dBm.

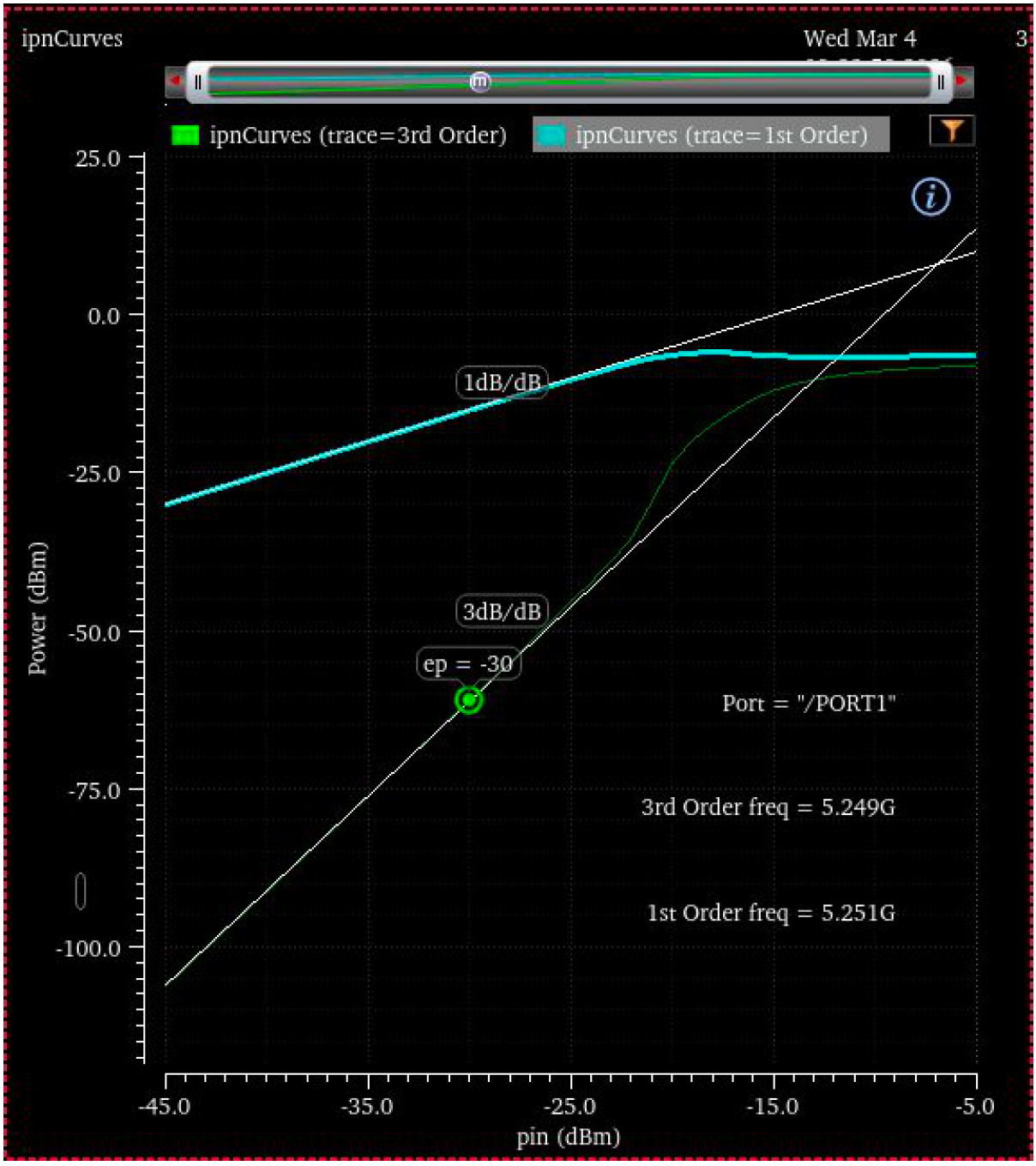


Fig 11. Input Intercept Point (3rd Order)

Figure 11 shows a measurement for the third order intermodulation intercept point. Although the graph says it was extrapolated at -30 dBm, my graph wouldn't update to my actual measurement extrapolating around -40 dBm for some reason. The reported value of -6.967 dBm represents the intercept point found by extrapolating from -40 dBm.

III. Design Methodology and First Pass Calculations

A. Output network

We first want to find usable values of inductance by simulating the Pi model inductor. We need to ensure that at whatever L value we choose, the self-resonant frequency (when Q = 0) is well above the operating frequency of 5.25 GHz.

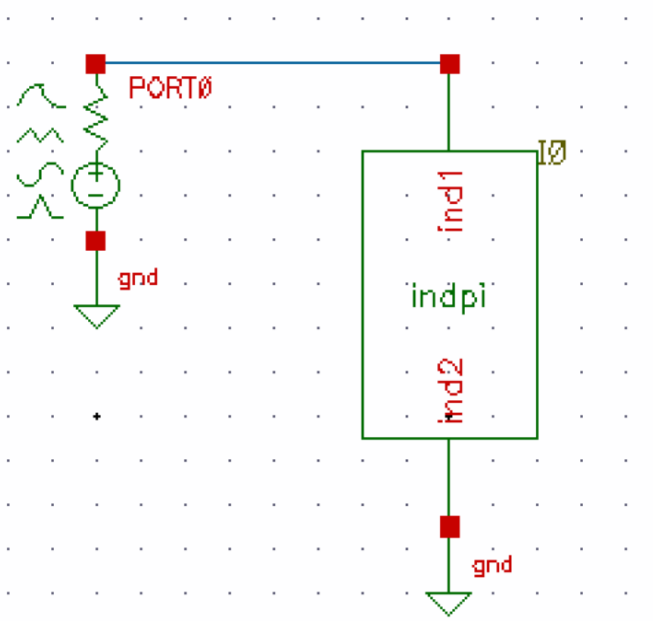


Fig 12. Pi Model Inductor Testbench

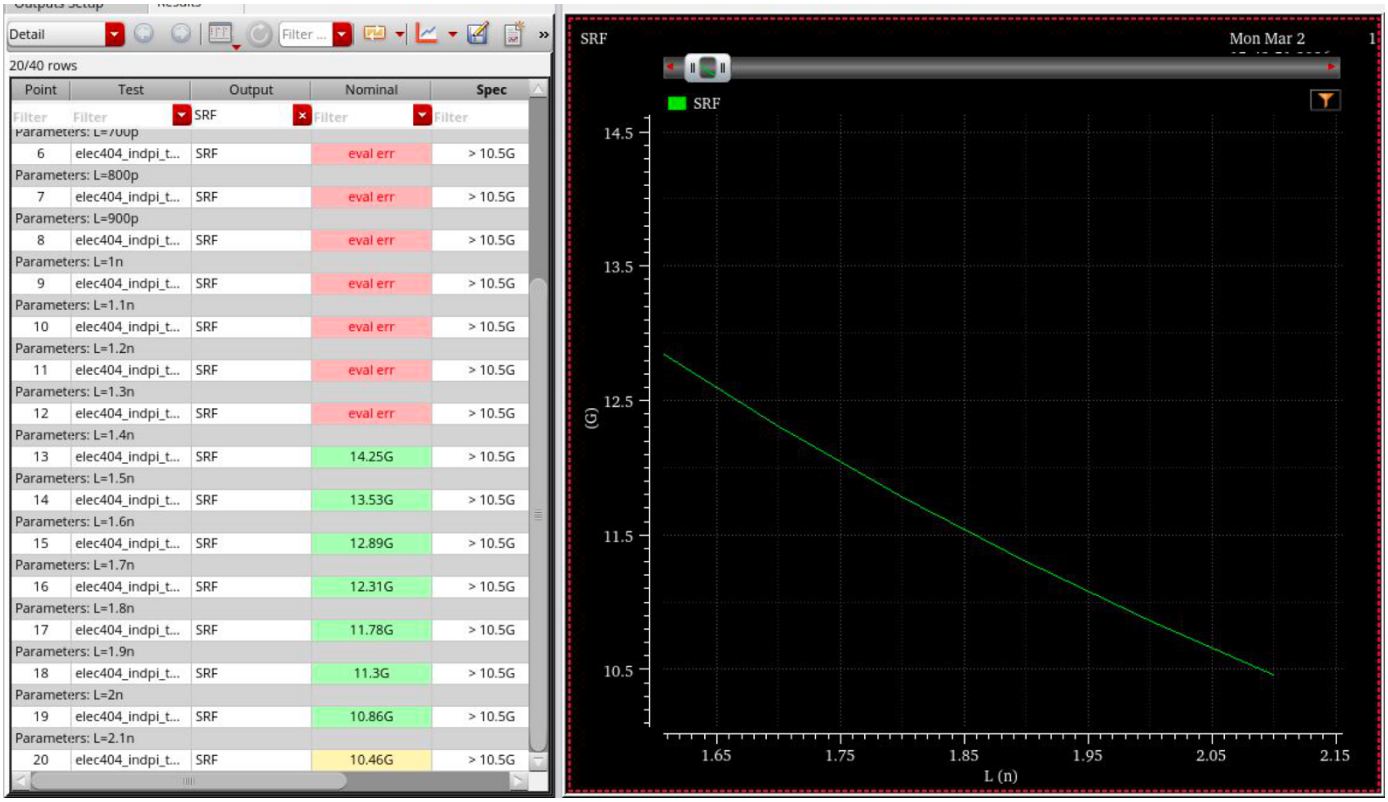


Fig 13. SRF vs L

In Figure 13, we can see that inductances below **2.1 nH** will have a self-resonant frequency above 10.5 GHz so the inductor will actually act like an inductor while the LNA operates. This value is good to keep in mind for Ld and Ls as they have AC ground on one end.

The output network can be transformed to be a parallel RLC network. We want to maximize our gain so Rp = Rs*(1+Q^2) will probably need to be maximized, while making sure the L will still act like an inductor below 10.5 GHz. Rp ended up being around 800 Ω.

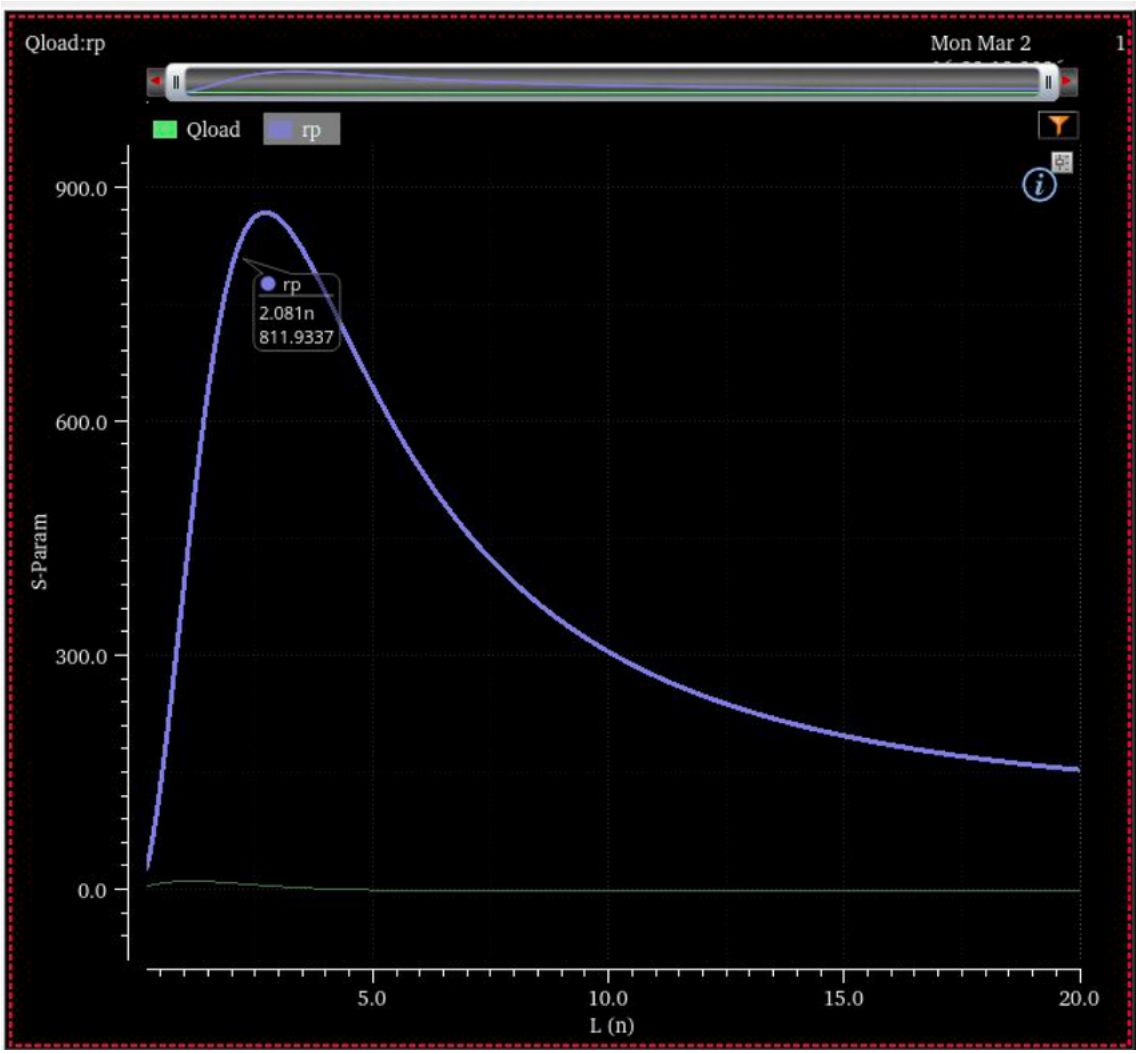


Fig 14. Rp vs L

One issue with the current network is that the output impedance won't match 50 Ω inputs that come after. In order to do that we create a tapped capacitor matching network. However, with some rough calculations in Figure 15, we find that we need more degrees of freedom to successfully match our network. So we might want to add another capacitor in parallel with the load.

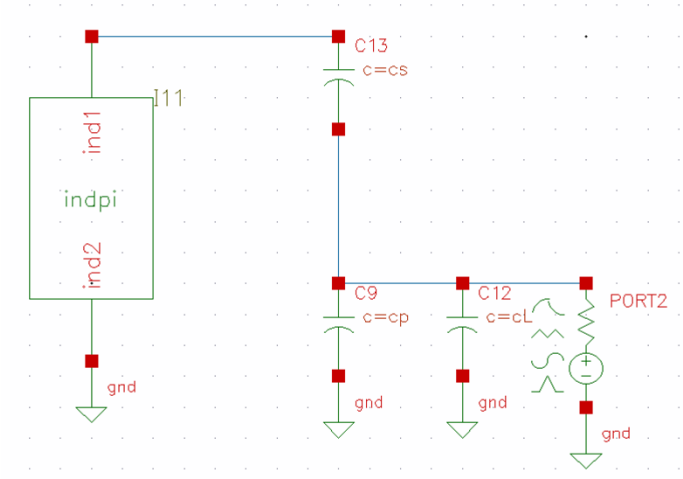


Fig 15. Output Impedance Matching Network

We need to make sure the real part of the impedance is 50 Ω and the reactive part of the impedance is 0 at the operating frequency 5.25 GHz. We can sweep Cs and Cp to search for the correct intercept points.

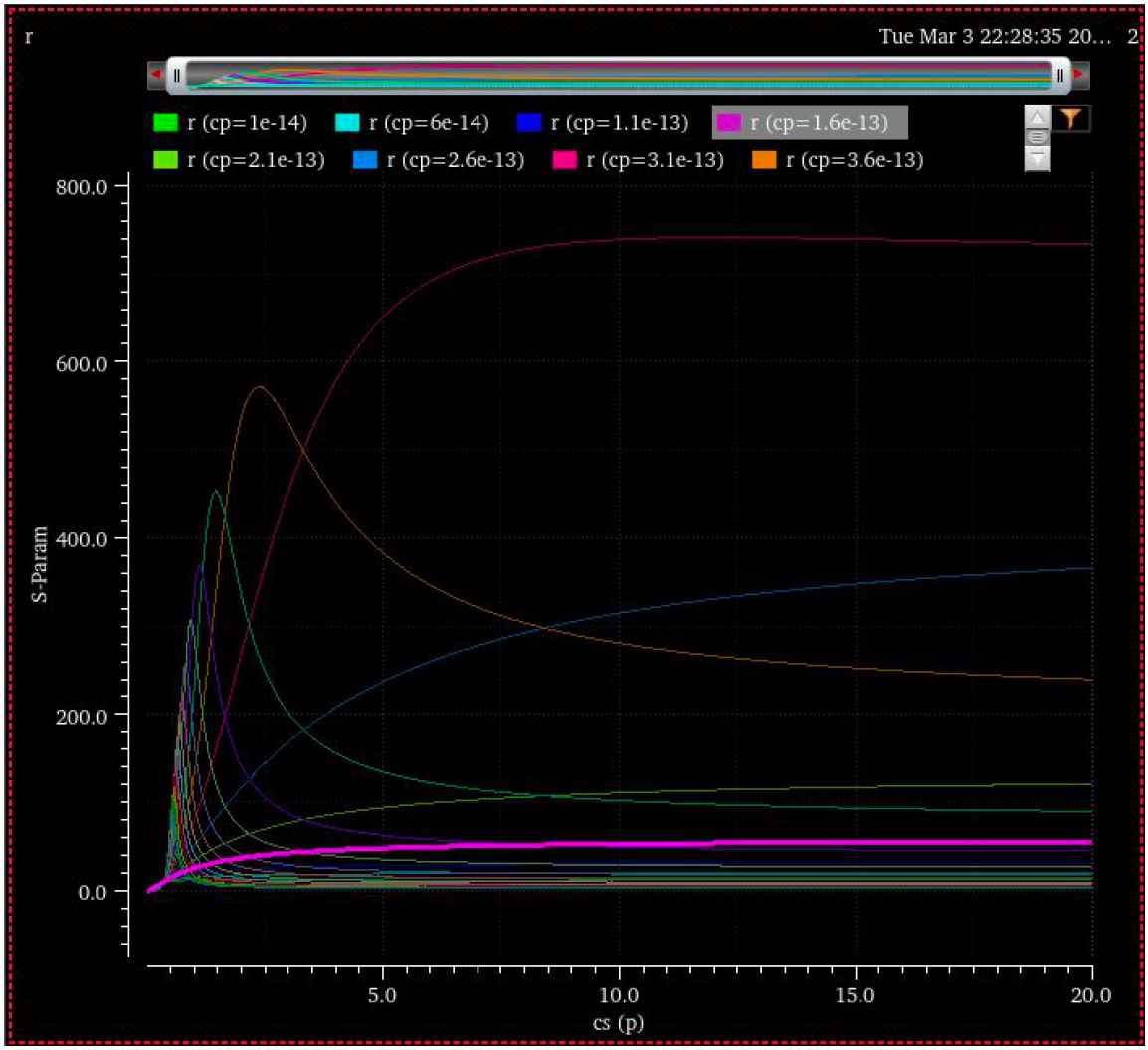


Fig 16. R vs Cs for different Cp values

In Figure 16, we find sweeping Cs, Cp needs to be > ~160 fF to have R = 50.

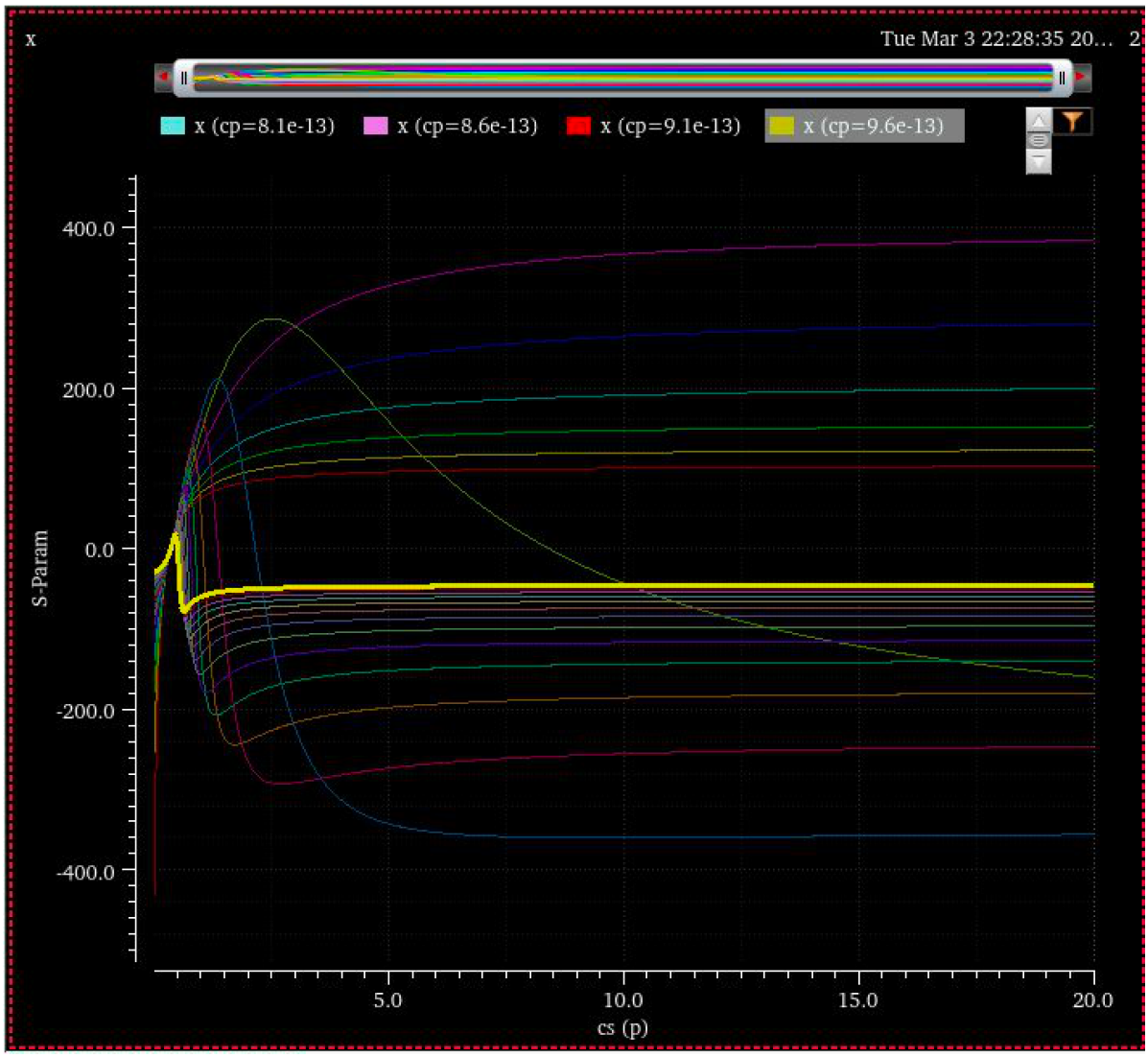


Fig 17. X vs Cs for different Cp values

In Figure 17, we find sweeping cs, almost any cp seems to have a zero crossing for X.

Graphing extracting the Cs values where R = 50 and X = 50 for every Cp, we just need to find when the values intersect. This ends up being around **Cp = 1.193 pF** and **Cs = 452.3 fF**.

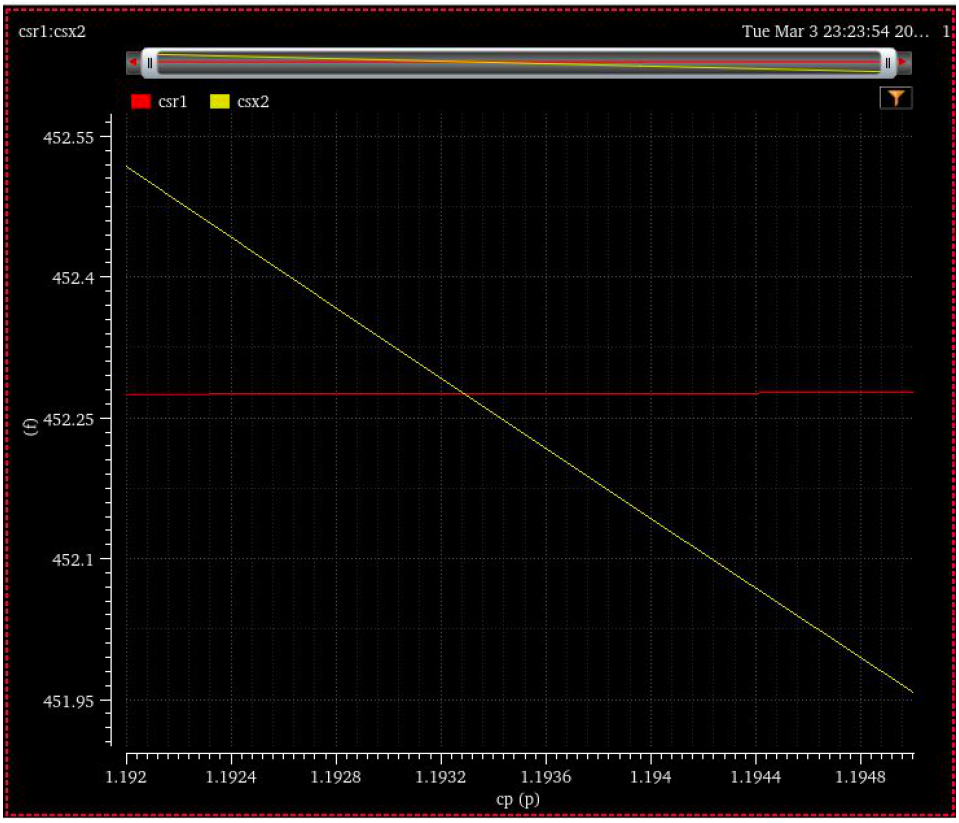


Fig 18. Intersect of Cs values where R = 50 and X = 0

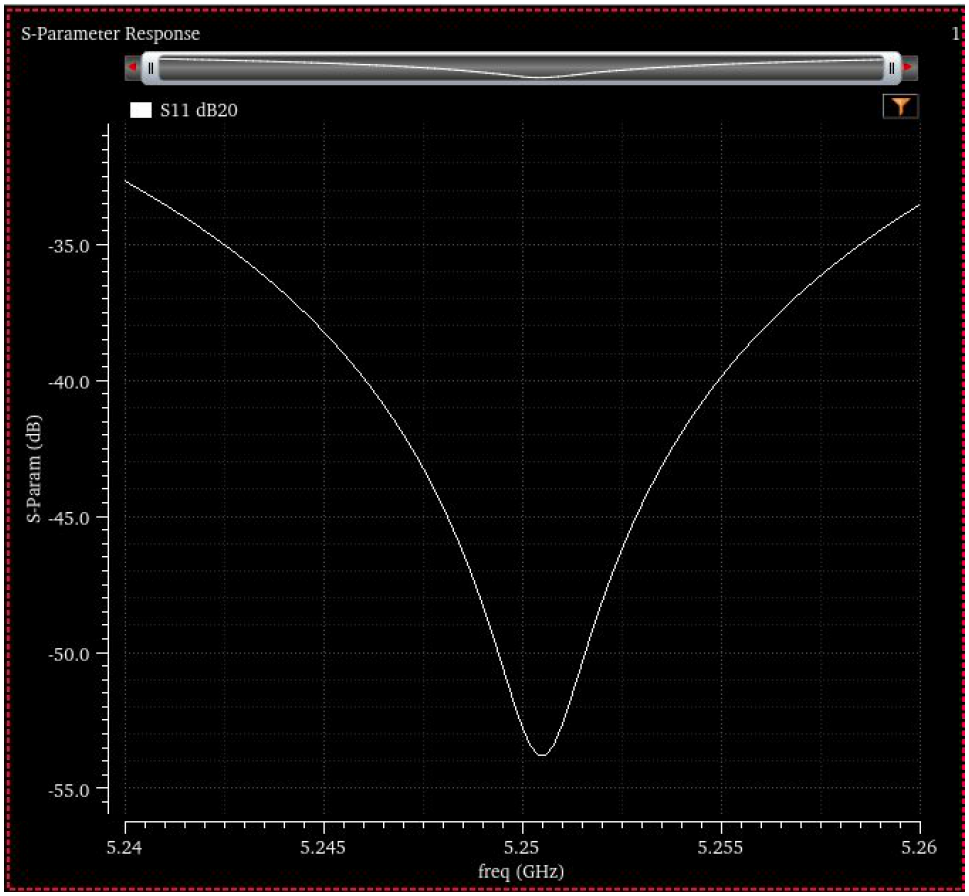


Fig 19. S22 of Output Network

B. Input network

We want to minimize Noise Figure. This quantity depends on something like $1+ f_{op}/f_{transit}$*(SN) where SN is a function of Qin and process variables. Since we aren't modelling gate induced noise SN is minimized with largest Qin. Maximising Qin reduces F (good), maximizes gain (good), but this reduces linearity (bad), and reduces bandwidth (bad). To achieve bandwidth spec of 200 MHz, Qin = f_{op}/BW = 26.25 which seems way to high.

Qin = 1/(ω_{op} *Cgs)/(Rs + $\omega_{transit}$ *Ls) and assuming everything is impedance matched, Qin = 1/(2* ω_{op} *Rs*Cgs). Simulating an NMOS transistor (we can assume W = 1 um, L = 45n to start with), we can find $\omega_{transit}$ but this line of reasoning leads to an Ls = 0.09 nH < 0.2 nH which is below our minimum. So instead, we start with **Ls = 0.2 nH** and find $\omega_{transit}$ with Rs = 50 = ωLs. We end up with f_t = 40 GHz. This transit frequency is very low so we needed an external capacitor to since 2*pi*f_t = gm/(Cgs + Cgd + Cext) since changing the transistor width affects both Cgs and gm at the same time. Adding **Cext = ~ 40 fF** made the frequency low enough and using this value we can sweep width until gm=19.6 mS, Cgs=30 fF_internal, Cgd match correctly. This ended up being around **50 um**. Since the Cgs values are parallel we have Cgs,eff = Cext + Cgs_internal = 70 fF.

To find Qin, we use Qin = 1/(2* ω_{op} *Rs*Cgs) = 4.3 and find **Lg = 10 nH** from ω_{op} = 1/sqrt[Cgs,eff*(Lg + Ls)] for resonance.

C. First Pass Values

TABLE 3
First Pass Values found from Hand Calculations

Vbias1	0.75 V
Vbias2	1.0 V
Cext	40 fF
Cp	**1.190 pF**
Cs	450 fF
Ld	2 nH
Lg	10 nH
Ls	0.2 nH
NM0 W/L	50*(1u/45n)
NM1 W/L	50*(1u/45n)

IV. Power Consumption Optimization

A. Initial Power Consumption

The initial design targeted 5 mA current (8 mW power) based on gain and linearity requirements. However, optimization was performed to reduce power while maintaining specifications.

B. Optimization Techniques

Several techniques were employed to minimize power consumption:

Transistor sizing optimization: The width of M0 was iteratively reduced from 150 μm to 125 μm while monitoring gain and noise figure. This reduced current from 5 mA to 2.8mA.

Biasing optimization: The gate bias voltage of M0 was adjusted to operate at lower current density while maintaining g_m sufficient for gain requirements.

Supply voltage consideration: Although VDD is fixed at 1.0V, the voltage headroom was optimized by adjusting the drain voltage of M1 to allow maximum signal swing with minimum current.

Inductor quality factor: Higher Q inductors reduce losses, allowing lower current for the same gain. Layout techniques were considered to maximize inductor Q.

C. Design Trade-offs

During optimization, several trade-offs were encountered:

Gain vs. Power: Reducing current directly impacts g_m and therefore gain. However, by maintaining g_m/I ratio near peak f_t, gain degradation was minimized.

Noise Figure vs. Power: Operating at lower current density increases noise figure. The optimal point was found at approximately 0.3 mA/μm where noise figure remained below 2.2 dB.

Linearity vs. Power: Lower bias current typically degrades IIP3. The final bias point maintains sufficient overdrive voltage to meet IIP3 requirements.

D. Final Power Consumption

Through the iterative optimization, the final design achieved 2.862 mW.

V. Conclusion

A fully-integrated CMOS low noise amplifier for 5.25 GHz wireless applications has been successfully designed, analyzed, and simulated using 45nm PDK models with a 1.0V supply voltage. The inductively-degenerated cascode topology was selected to achieve the required performance metrics while maintaining stability and reverse isolation. Through systematic hand calculations and iterative simulation-based optimization, the LNA meets or exceeds all specified requirements: input return loss of -10.6 dB, output return loss of -13.7 dB, reverse isolation better than -41.5 dB, forward gain of 15.3 dB, noise figure of 2.003 dB, and IIP3 of -6.967 dBm across the 200 MHz bandwidth centered at 5.25 GHz. Particular attention was given to power consumption optimization, resulting in a final power dissipation of only 2.862 mW achieved through careful transistor sizing, biasing optimization, and trade-off management between gain, noise figure, and linearity. The output matching network was precisely designed using a tapped capacitor approach to interface with the 50 fF load capacitance, while the input network was optimized for simultaneous power and noise matching. This design demonstrates that high-performance LNAs meeting stringent RF specifications can be realized in advanced CMOS technologies with minimal power consumption, making them suitable for modern wireless communication systems.